

# **Mixed-Signal Event-Driven Simulation of a Phase-Locked Loop**

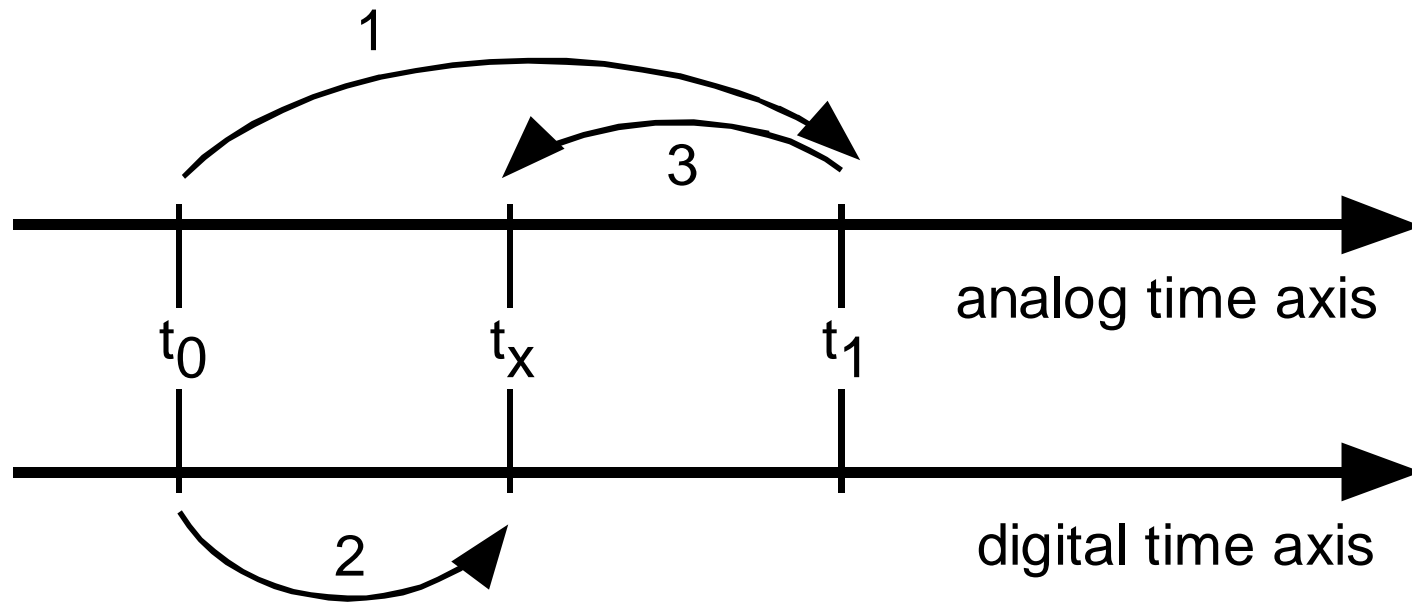
Prof. Dr. Martin Schubert

# Outline

- Basics of the Mixed-signal Event-Driven (MixED) Simulation Method
- Time Axis Considerations
- Problems of D/A Conversion
- Problems of A/D Conversion
  - + General Aspects of A/D Conversion
  - + Analog-In/Digital-out VCO as A/D Converter
- Applications: Digital Phase-Locked Loop (DPLL) Simulation Examples

# Double-Time Axis Problem

1. Analog kernel steps forward from  $t_0$  to  $t_1$
2. Digital kernel performs smaller step from  $t_0$  to  $t_x$  and triggers analog event
3. Backstepping of analog kernel from  $t_1$  to  $t_x$ .



# MixED Module: VHDL Time Axis

## Advantages:

- + 1 Time Axis
- + Fast A/D and D/A interaction
- + No backstepping

## Problems:

- No backstepping possible
- Careful setting of time points required!

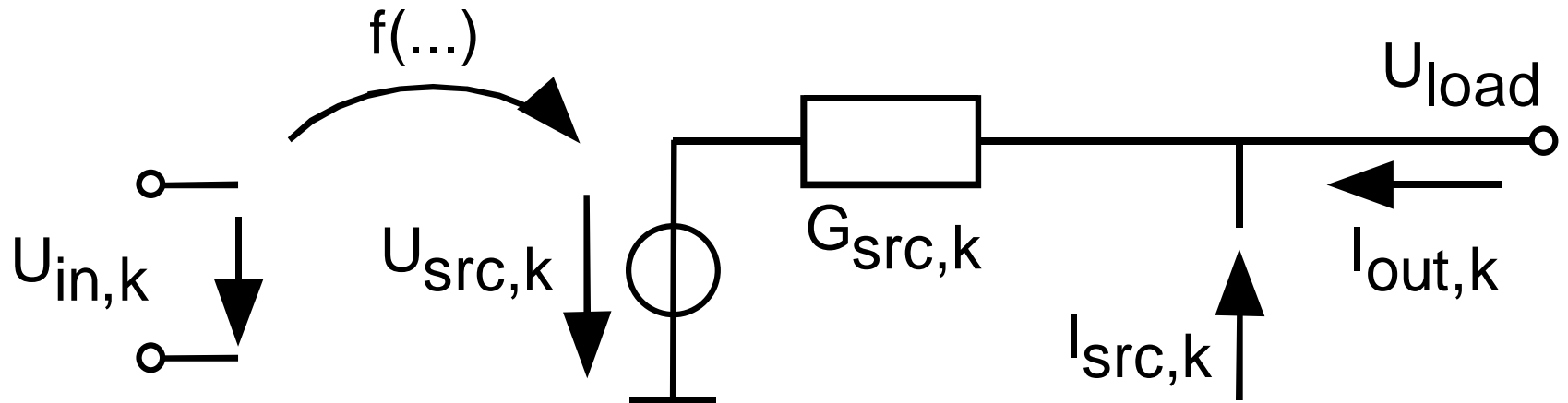
# VHDL Time Axis Features

- Standard VHDL: Defined resolution: 1 fs
- Typical simulator: resolution  $>1$  fs to increase maximum simulation time
- 1<sup>st</sup> action of MixED module:
  - + check resolution during initialization step
  - + make minimum step known to all MixED models via global parameter (VHDL record field named *gp.time\_resolution*)

# The Controlled Source Model

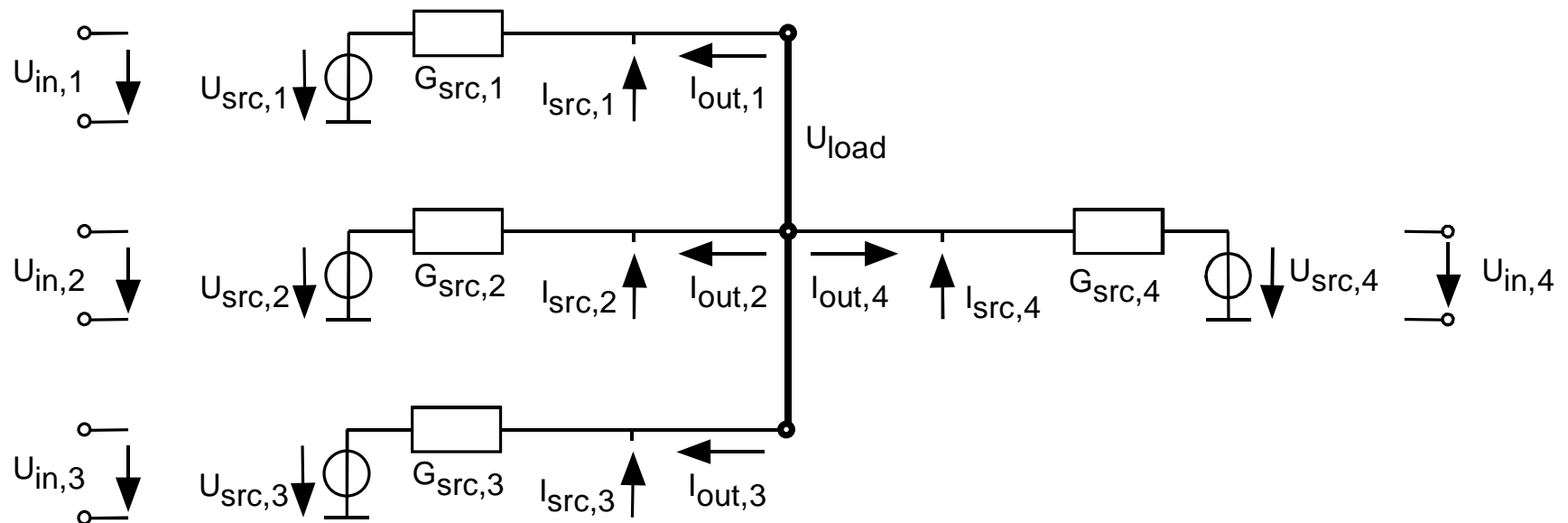
## Quantities:

Input:  $U_{in}$   
Intermediate:  $G_{src}, U_{src}, I_{src}$   
Output:  $U_{load}, I_{out}$

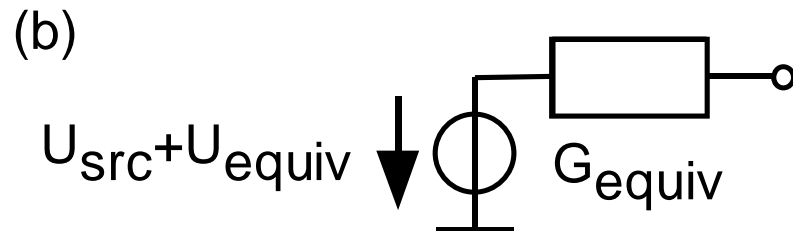
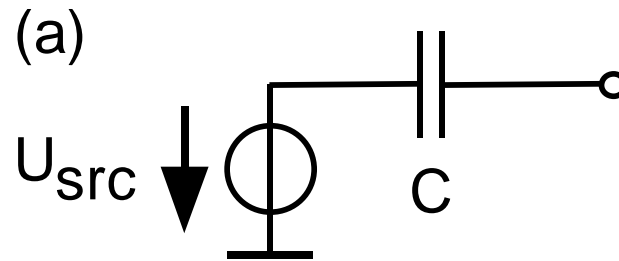


# Combining Several Source Elements

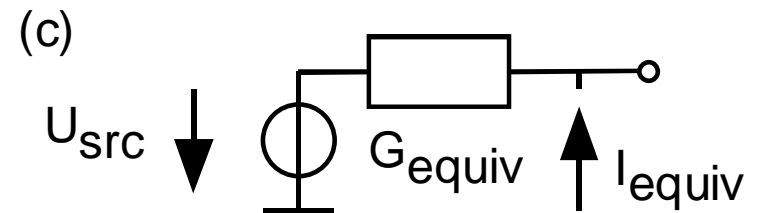
- One iteration solves the problem for one node and linear devices
- Several iterations required for nonlinear devices (e.g. CMOS gates)



# Modeling a Capacitive Output Imp. with a Controlled Source Element

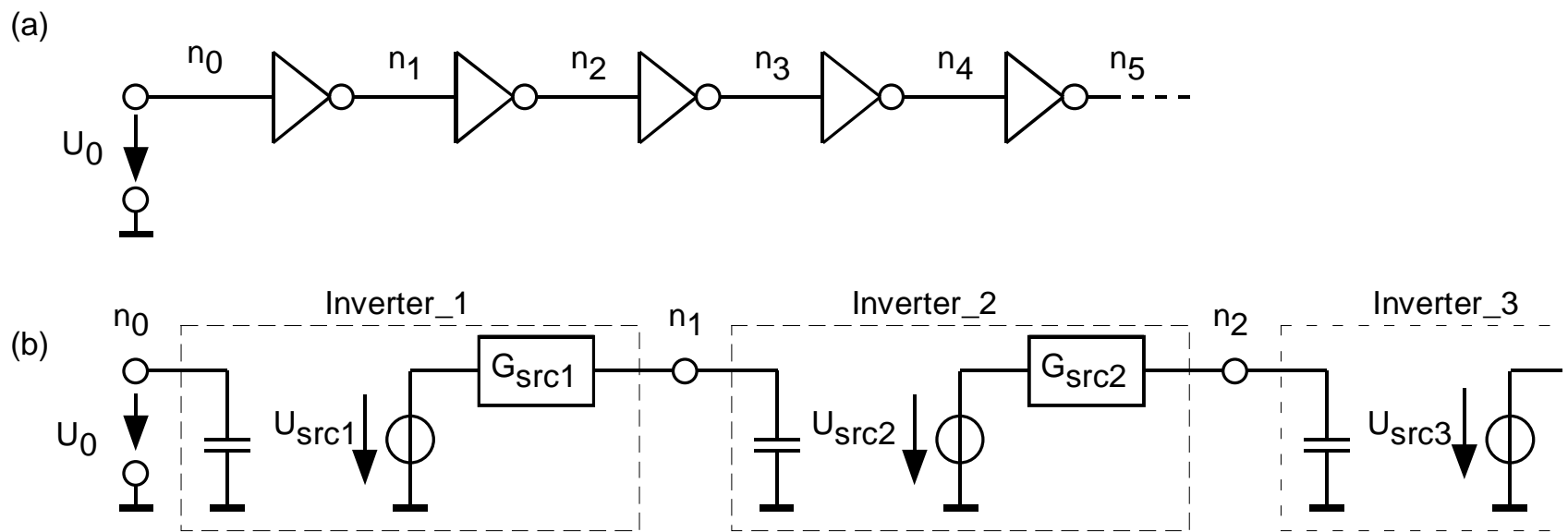


equivalent circuit with conductor and voltage source



equivalent circuit with conductor and current source

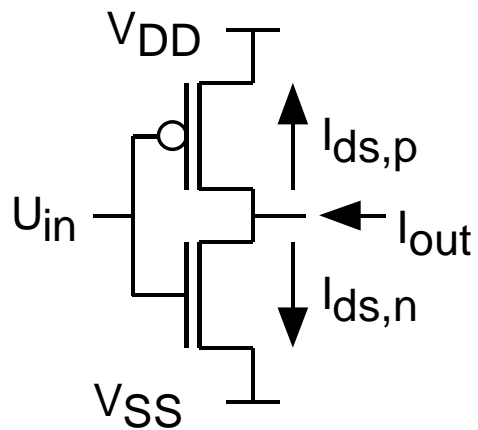
# Problems Suitable for MixED Simulation



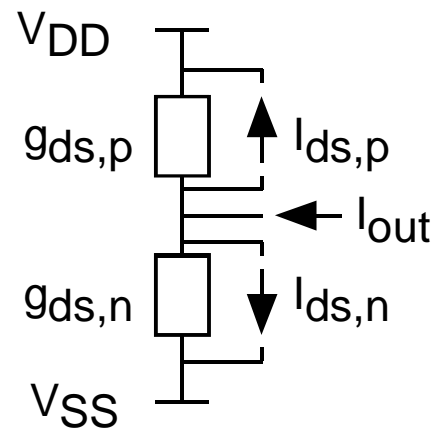


# Modeling a CMOS Inverter

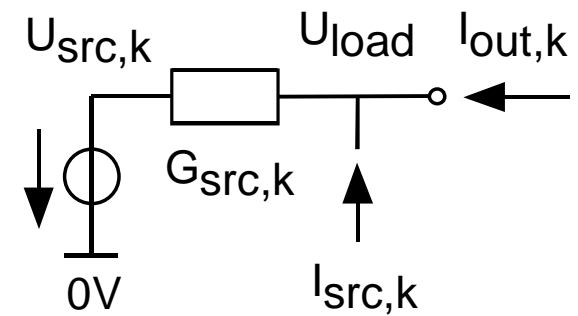
(a)



(b)



(c)



# Too Simple 1-Bit D/A Conversion

```
CONSTANT Vdd: REAL:=5.0; -- volts
```

```
CONSTANT Vss: REAL:=0.0; -- volts
```

```
SIGNAL logic_value: BIT;
```

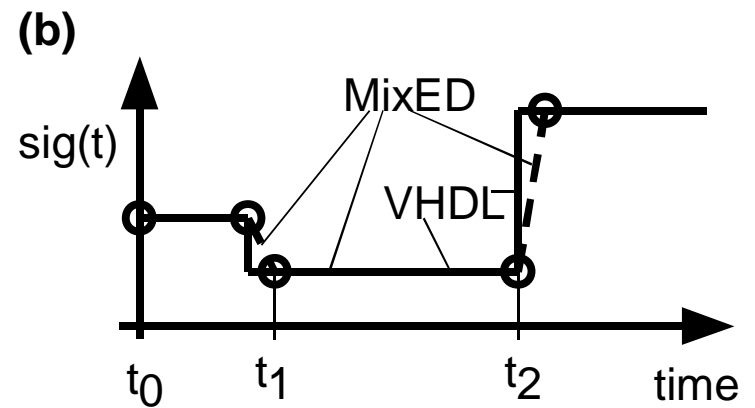
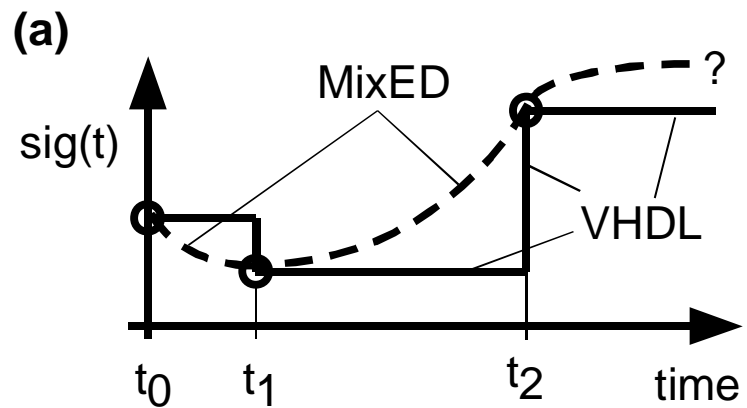
```
SIGNAL real_value: REAL;
```

```
...
```

```
real_value <= Vss WHEN logic_value = '0' ELSE Vdd;
```

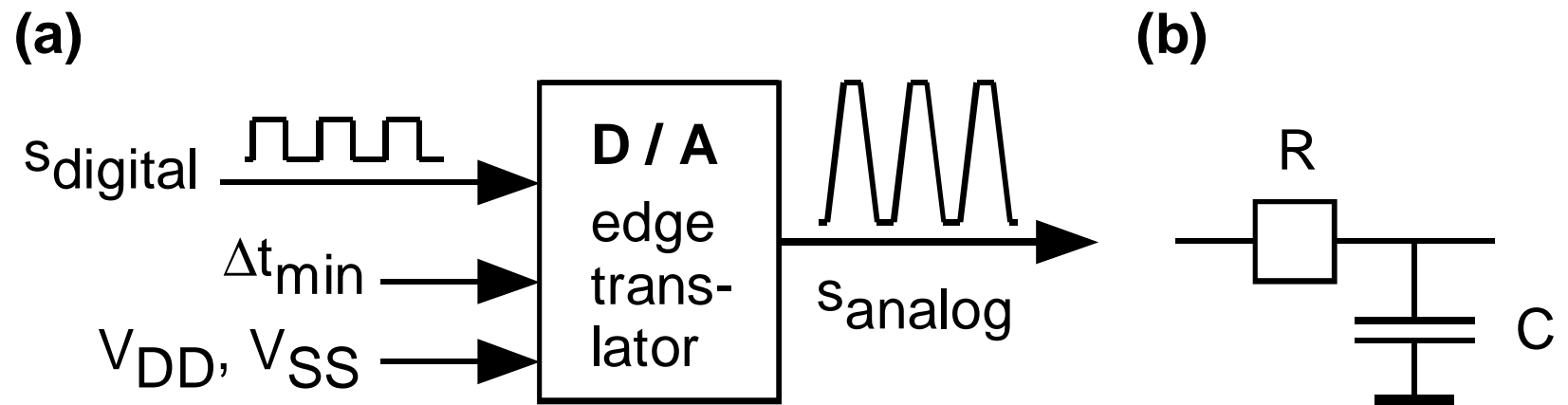
```
...
```

# Curve Interpretation of standard VHDL versus MixED Module



# General D/A Conversion

- Minimum width edges remove time stepping problem
- More natural edges can be obtained with appended circuitry



# Too Simple A/D Conversion

```
CONSTANT Uref: REAL:=2.5; -- volts
```

```
SIGNAL logic_value: BIT;
```

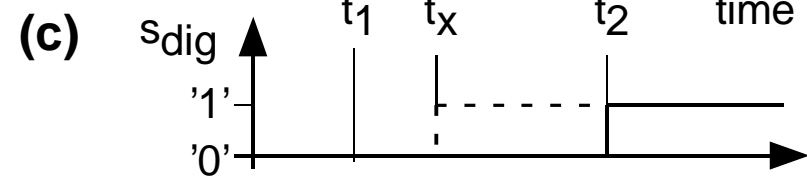
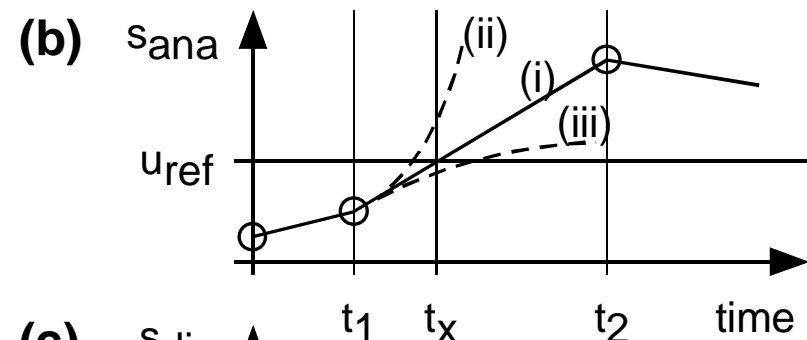
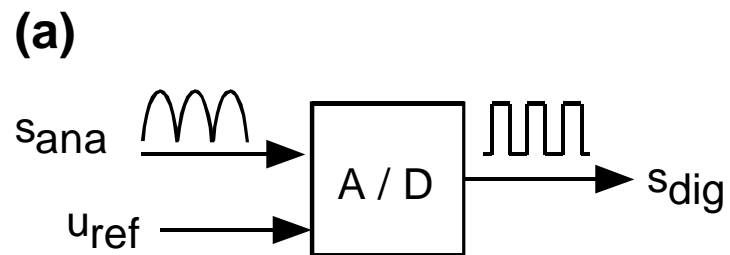
```
SIGNAL real_value: REAL;
```

```
...
```

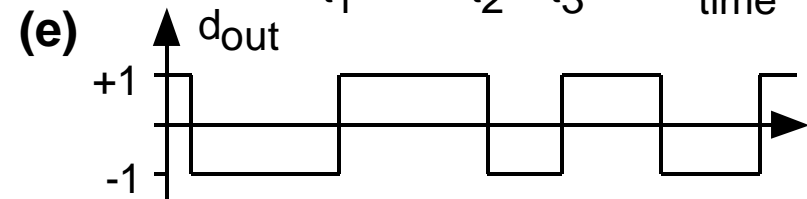
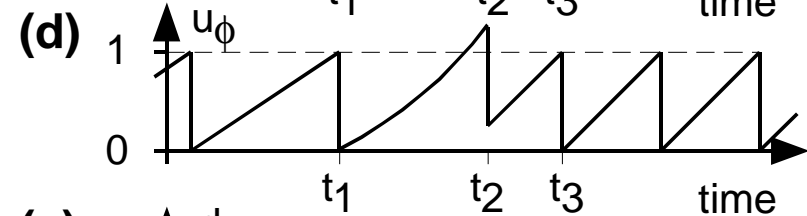
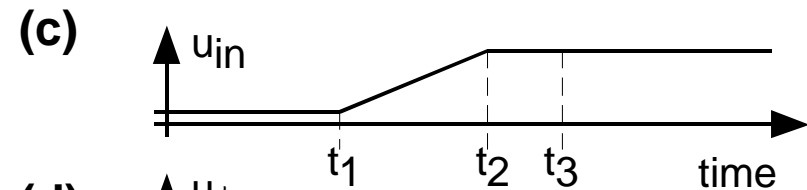
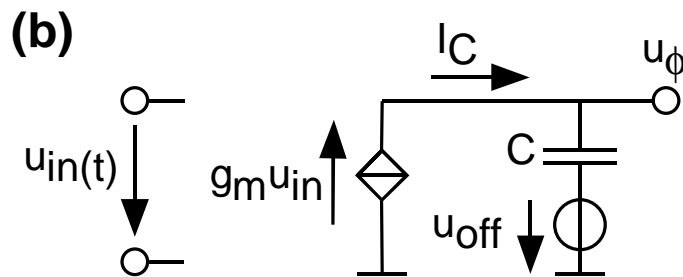
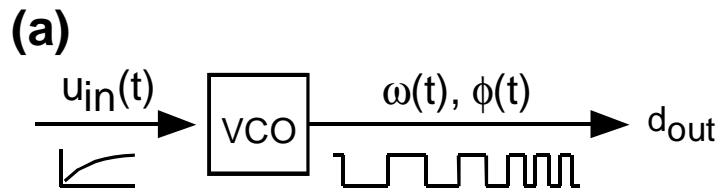
```
logic_value <= '0' WHEN real_value < Uref ELSE '1';
```

```
...
```

# Improved A/D Conversion



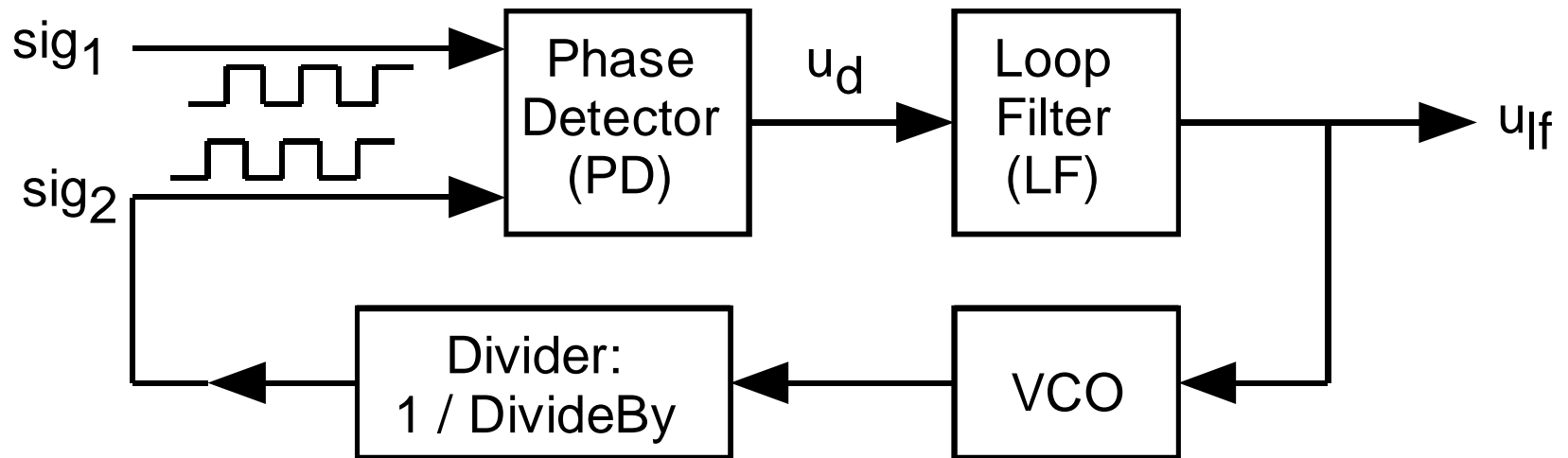
# A/D Conversion by Digital VCO



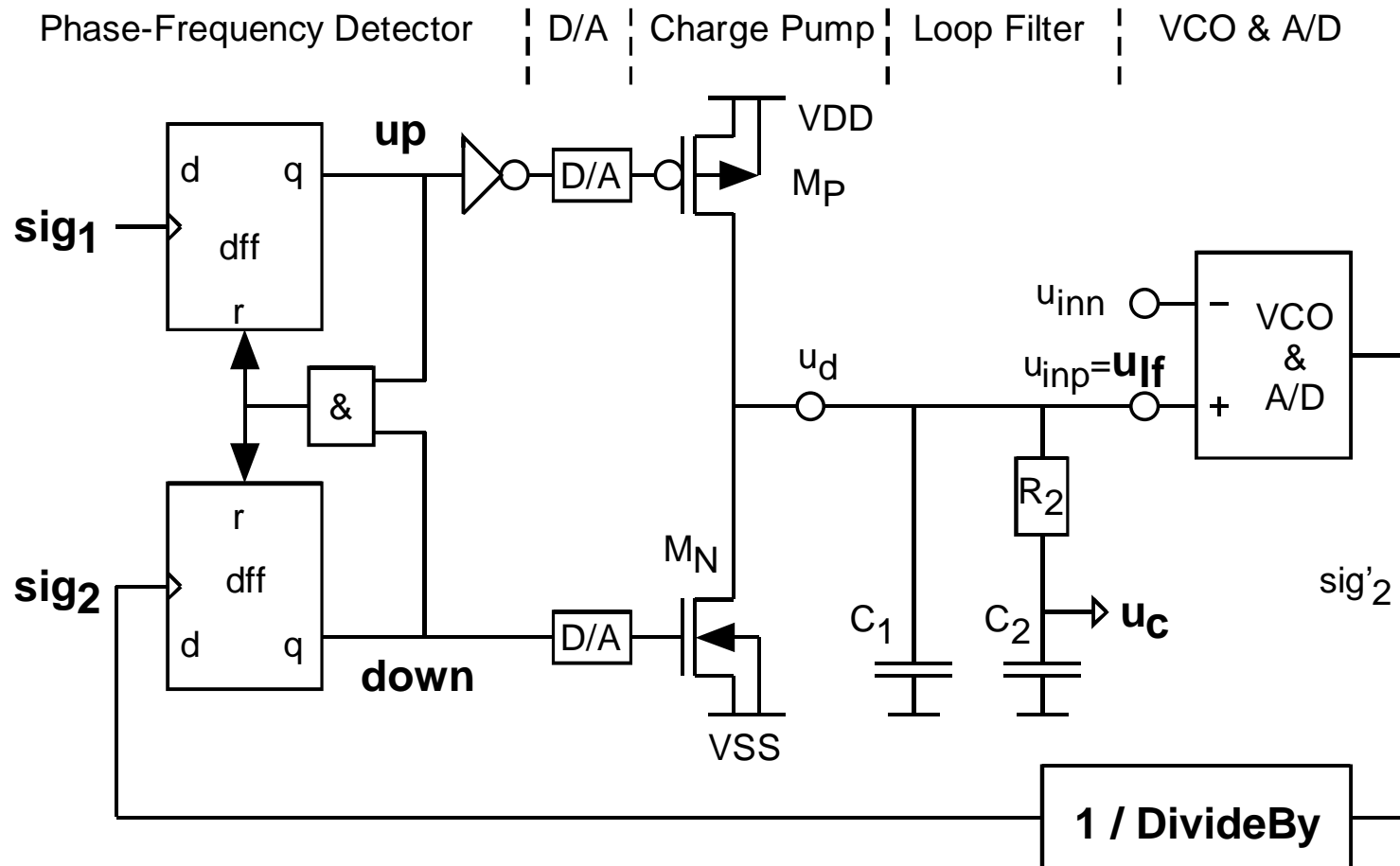
$$f_{VCO}(t) = K_{VCO} \cdot u_{in}(t) + f_{FR}$$

$$\phi_{VCO} = \int \omega_{VCO} dt = 2\pi K_{VCO} \int (u_{in}(t) + f_{FR}) dt$$

# Digital Phase-Locked Loop (DPLL) Block Diagram



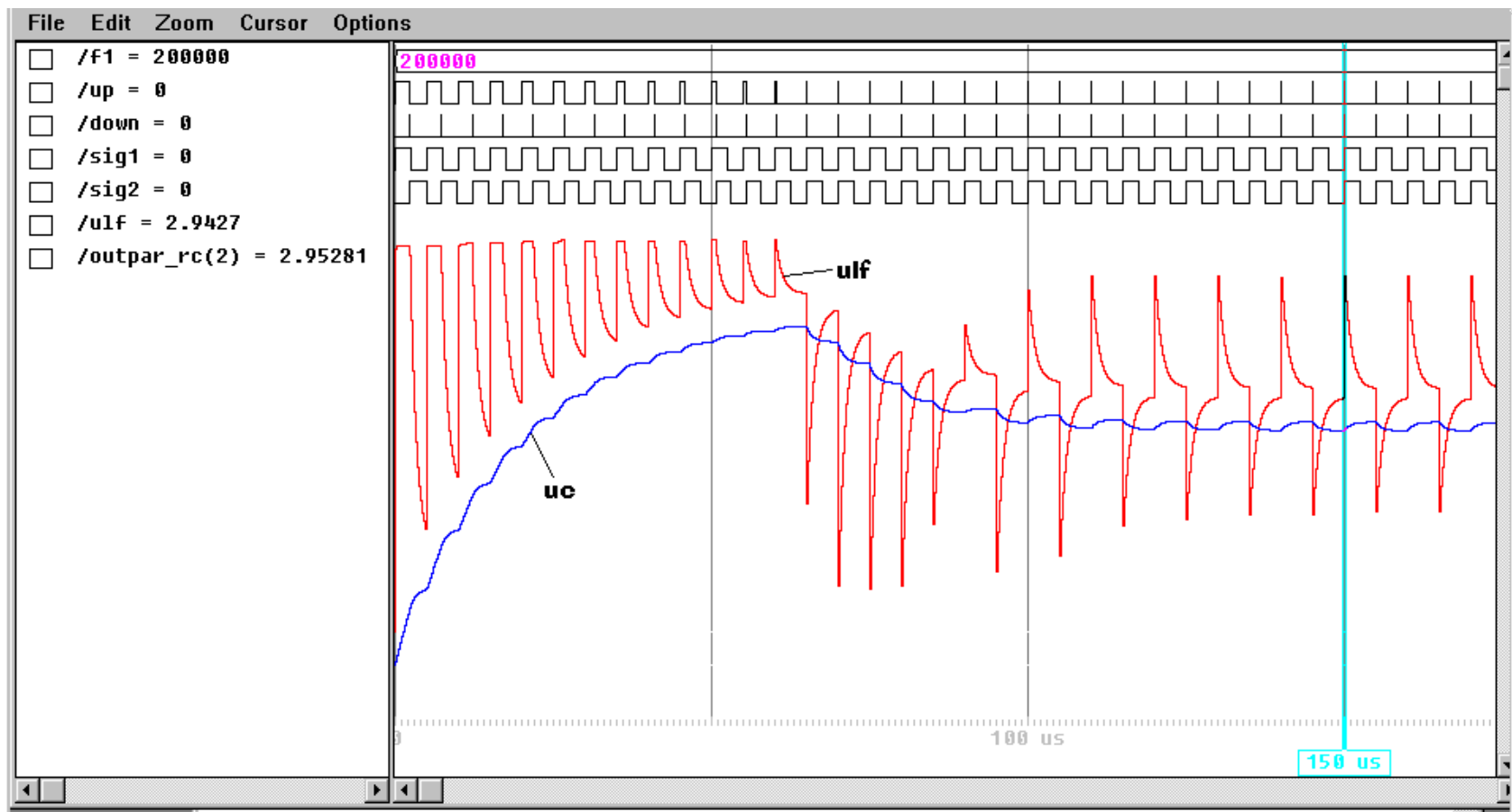
# Digital Phase-Locked Loop (DPLL) Schematics



# Mixed-Signal Simulation of DPLL

$t=0$ :  $u_{if}=u_c=0$ , Input:  $f(\text{sig}_1)=200 \text{ KHz}$ , VCO:  $f_{FR} = 200 \text{ KHz}$ ,  $K_{VCO} = 4.5 \text{ KHz/V}$ ,  $U_{inn} = 3\text{V}$

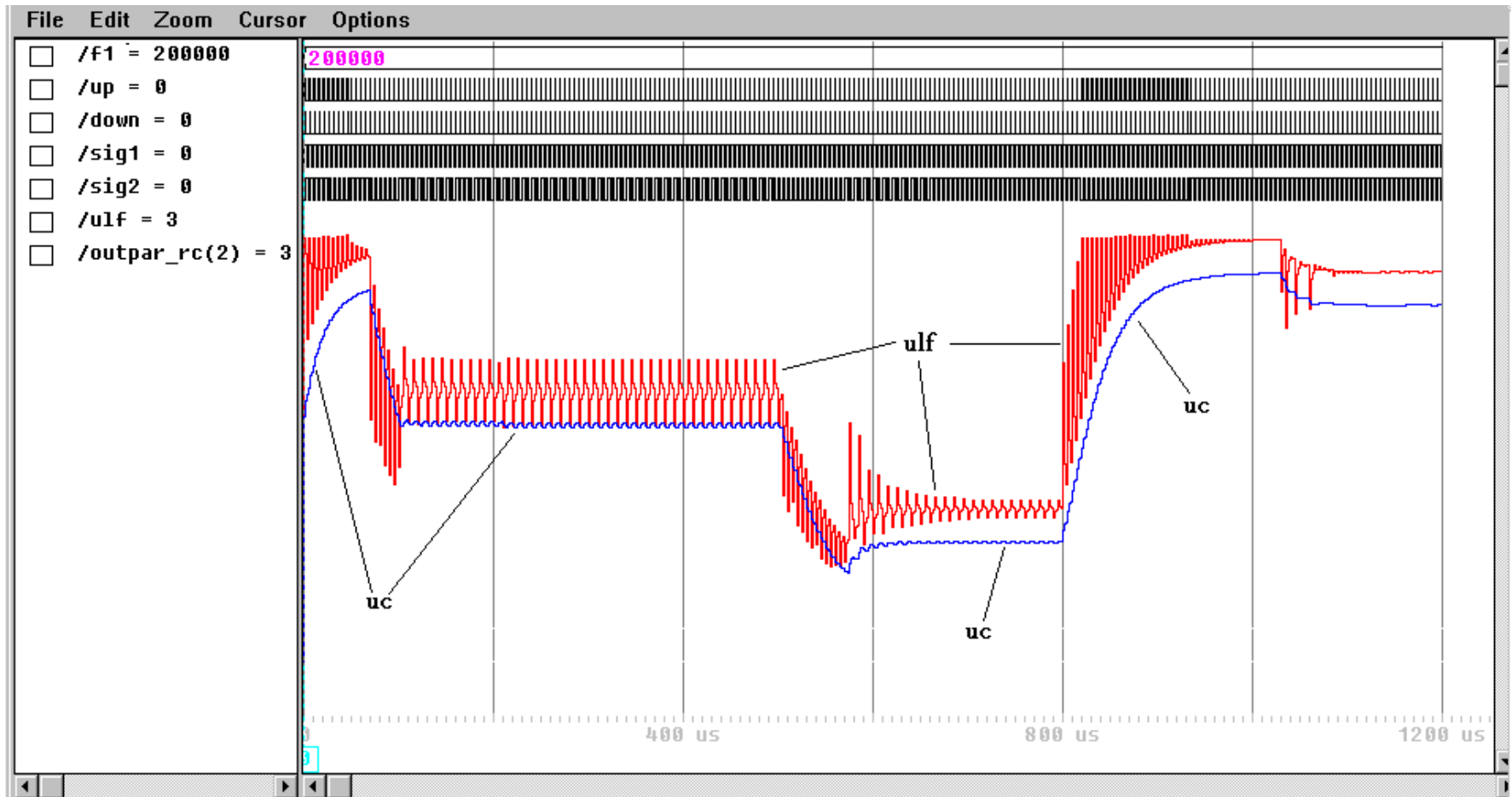
Divider is transparent:  $\text{DevideBy} \leq 1$ ;  $V_{SS}=0\text{V}$ ,  $V_{DD}=5\text{V}$ .



# Mixed-Signal Simulation of DPLL

$t=0$ :  $u_{if}=u_c=0$ , Input:  $f(\text{sig}_1)=200$  KHz, VCO:  $f_{FR} = 200$  KHz,  $K_{VCO} = 20$  MHz/V,  $U_{inn} = 3$  V

**Divider:** DivideBy  $\leq 4450$ , 4448 AFTER 200  $\mu$ s, 4300 AFTER 500  $\mu$ s, 4600 AFTER 800  $\mu$ s;



# Conclusion

- A limited range of analog and mixed signal devices can be simulated with standard VHDL.
- The DPLL, which is one of the most important mixed-signal building blocks in digital designs, can be modeled using standard VHDL and the MixED method