

Number of segments	4	8	10	13	19	25	30	40	50	60
Symbolic method (sec)	0.009	0.012	0.014	0.024	0.0336	0.0389	0.0456	0.077	0.13	0.17
SPICE (sec)	0.3	0.33	0.34	0.35	0.38	0.41	0.43	0.48	0.51	0.58
Speed-up	33	27.5	24.28	14.58	11.3	10.53	9.42	6.23	3.92	3.41

Table 1: Execution time for symbolic method and SPICE

sis. Because of its simplicity, we decided to implement the symbolic method using recursive function calls. However, this resulted in longer execution times. We believe that execution times can be significantly shortened if a symbolic expression tree is set-up for transient analysis. This would offer two advantages: (1) the avoidance of recursive calls, which are very cumbersome in terms of their execution time and (2) the possibility of reusing already computed symbol values in multiple places. A more time-effective implementation of the suggested transient analysis method can be subject for future research.

## 4 Conclusion

This paper presents a novel symbolic analysis method for transient analysis of DSN propagation. The method relies on symbolic techniques to express the voltage variations at the power pins of analog blocks depending on the DSN (described as current variations) at switching digital blocks. The paper discusses the modeling of the DSN propagation to the power pins of analog blocks. This includes the representation of the substrate coupling, contacts to the power supplies and power buses. Our experimental results support the correctness of the calculated DSN values as compared to SPICE simulations. Besides, we showed that the method offers significant speed-ups as related to traditional SPICE simulation times.

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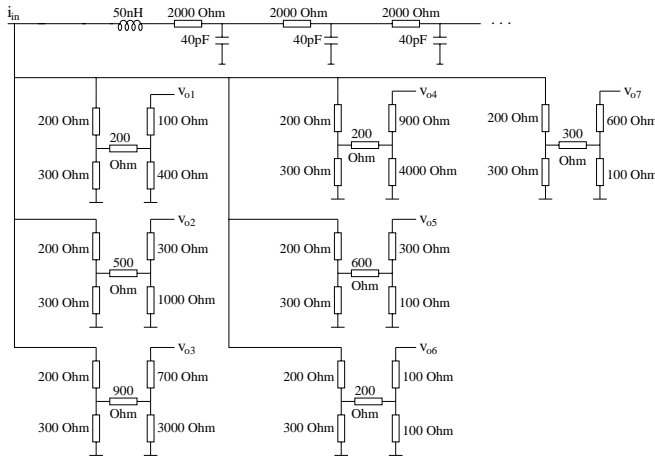


Figure 6: **Experimental set-up for the transient analysis method**

parameters of the composing blocks are needed for calculating parameter  $a_{21}$ . Also, each meta-node includes a field that points to a symbolic expression tree that describes how parameters of composing blocks relate to the parameter denoted by the meta-node. Note that these expression trees can be shared among parameters. We mathematically proved that such sharings result in PMs of polynomial size, in the general case. This determines a significant PM size reduction as it is well known that symbolic models are of exponential size in the general case [10].

Symbolic PMs can be numerically evaluated for finding DSN values. Power net routing and sizing fixes the  $R$  and  $C$  values of the segments that form the power net. Next, DSN can be computed by traversing the DSN PM and performing the computations expressed through the expression trees. Experiments showed that numerical evaluation of symbolic PMs is significantly faster than SPICE and offers same accuracy.

### 3 Experimental Results

The symbolic transient analysis methods were implemented as about 700 lines of C code. The experimental set-up for the proposed symbolic transient method addresses two aspects: (1) the correctness of the method and (2) its execution time. For experimental purposes, we used the circuit depicted in Figure 6. The circuit includes a number of identical RC stages which model the power bus and seven similar resistor structures that model the substrate couplings between one digital noise source and the power pins of seven analog blocks. Current  $i_{in}$  is produced by a current source that models the DSN generated by the switching digital block. Voltages  $v_{o1}$ ,  $v_{o2}$ , ...,  $v_{o7}$  are the variations at the analog power pins due to the DSN  $i_{in}$ . The digital power bus included 10 segments.

Figures 7 present the voltage  $v_{o1}$  calculated using our symbolic transient method and using SPICE. Similar results were obtained for the other voltages, also. The Fig-

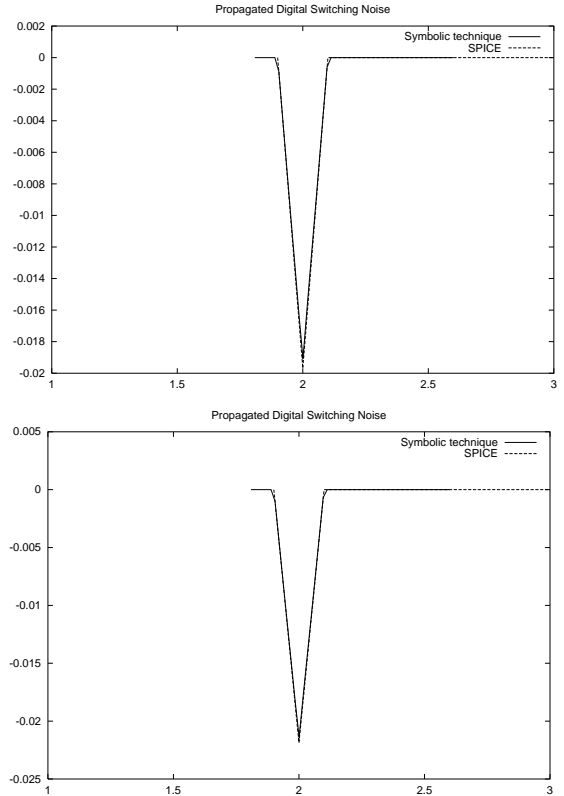


Figure 7: **Variations of voltages  $v_{o1}$  and  $v_{o2}$**

ures show that our technique is correct and it provides results within a very small relative error (less than 1%) from the values calculated with SPICE.

The second experiment studied the execution time of the proposed symbolic method and compared it against SPICE simulation times. For automated, exploration-based synthesis, this is a very important issue because evaluation (simulation) time has to be as small as possible in order to guarantee that a high number of solution points are evaluated. In order to study the execution time, we varied the size of the analyzed (simulated) models by changing the number of segments that compose the digital power bus.

Figure 1 presents the resulted execution times for our symbolic transient analysis method and for SPICE. For each experiment, the obtained speed-up (defined as SPICE simulation time over symbolic transient analysis execution time) is also indicated. The execution time of the suggested transient analysis method is in all cases smaller than the SPICE simulation time. Resulting speed-ups differ from about 25 times for shorter power buses to about 3.4 times for longer power buses. The reason for the speed-up decrease with the increase of the power bus length is the implementation method adopted for transient analy-

needed to replace a set of two connected blocks with a composed block. Composing blocks can be either RC stages or other previously composed blocks. Figure 4(b) shows the composition of two RC stages into a single composed block. Note that this composition generates a four-port block: two physical ports (described by current-voltage pair) and two virtual ports for the two state-variables of the composed block. Hence, each composition step (that involves an RC stage and another RC stage or a composed block) increases by one the number of ports of the composed block. As Figure 4(c) shows, after  $i$  composition steps, the composed block has  $i + 2$  ports (two physical ports and  $i$  virtual ports). To characterize a new composition step, the matrix parameters of the overall block with  $i+3$  ports must be related to the parameters of its two composing blocks (one with  $i + 2$  ports and the second with three ports). Parameters  $DPB^{l,j}$  of a digital power net composed of  $n$  RC segments (or parameters  $APB^{l,j}$  of an analog power net formed of  $k$  RC segments) can be calculated by applying recursively the composition rule  $n$  ( $k$ ) times.

For Figure 4(c), the following equation set results by applying the definition of the block matrices:

$$\begin{aligned}
v_1(t) &= a_{11}i_1(t) + a_{12}q_1(t-1) + a_{13}q_2(t-1) \dots a_{1,i+1}q_i(t-1) + a_{1,i+2}i_x \\
q_1(t) &= a_{21}i_1(t) + a_{22}q_1(t-1) + a_{23}q_2(t-1) \dots a_{2,i+1}q_i(t-1) + a_{2,i+2}i_x \\
q_2(t) &= a_{31}i_1(t) + a_{32}q_1(t-1) + a_{33}q_2(t-1) \dots a_{3,i+1}q_i(t-1) + a_{3,i+2}i_x \\
&\dots \\
q_i(t) &= a_{i+1,1}i_1(t) + a_{i+1,2}q_1(t-1) + a_{i+1,3}q_2(t-1) \dots a_{i+1,i+1}q_i(t-1) + a_{i+2,i+2}i_x \\
v_x(t) &= a_{i+2,1}i_1(t) + a_{i+2,2}q_1(t-1) + a_{i+2,3}q_2(t-1) \dots a_{i+2,i+1}q_i(t-1) + a_{i+2,i+2}i_x \\
v_2(t) &= b_{11}i_2(t) + b_{12}Q(t-1) + b_{13}v_x(t) \\
Q(t) &= b_{21}i_2(t) + b_{22}Q(t-1) + b_{23}v_x(t) \\
i_x(t) &= b_{31}i_2(t) + b_{32}Q(t-1) + b_{33}v_x(t)
\end{aligned}$$

Next, unknowns  $v_x$  and  $i_x$  are eliminated from the equation set and corresponding terms are identified with the terms that characterize the composed block. The following relationships, that also constitute the general composition rule, resulted after these mathematical manipulations of the equation set:

$$\begin{aligned}
a_{m,l}^{res} &= a_{m,l} + a_{m,i+2} \frac{a_{i+2,l}b_{33}}{1 - a_{i+2,i+2}b_{33}}, \text{ for } m = 1, i+1 \text{ and } l = 1, i+1 \\
a_{m,i+2}^{res} &= \frac{a_{m,i+2}b_{31}}{1 - a_{i+2,i+2}b_{33}}, \text{ for } m = 1, i+1 \\
a_{m,i+3}^{res} &= \frac{a_{m,i+3}b_{32}}{1 - a_{i+2,i+2}b_{33}}, \text{ for } m = 1, i+1 \\
a_{i+2,l}^{res} &= \frac{a_{i+2,l}b_{13}}{1 - a_{i+2,i+2}b_{33}}, \text{ for } l = 1, i+1 \\
a_{i+2,i+2}^{res} &= b_{11} + b_{13} \frac{a_{i+2,i+2}b_{31}}{1 - a_{i+2,i+2}b_{33}} \\
a_{i+2,i+3}^{res} &= b_{12} + b_{13} \frac{a_{i+2,i+2}b_{32}}{1 - a_{i+2,i+2}b_{33}} \\
a_{i+3,l}^{res} &= \frac{a_{i+2,l}b_{23}}{1 - a_{i+2,i+2}b_{33}}, \text{ for } l = 1, i+1 \\
a_{i+3,i+2}^{res} &= b_{21} + b_{23} \frac{a_{i+2,i+2}b_{31}}{1 - a_{i+2,i+2}b_{33}} \\
a_{i+3,i+3}^{res} &= b_{22} + b_{23} \frac{a_{i+2,i+2}b_{32}}{1 - a_{i+2,i+2}b_{33}}
\end{aligned}$$

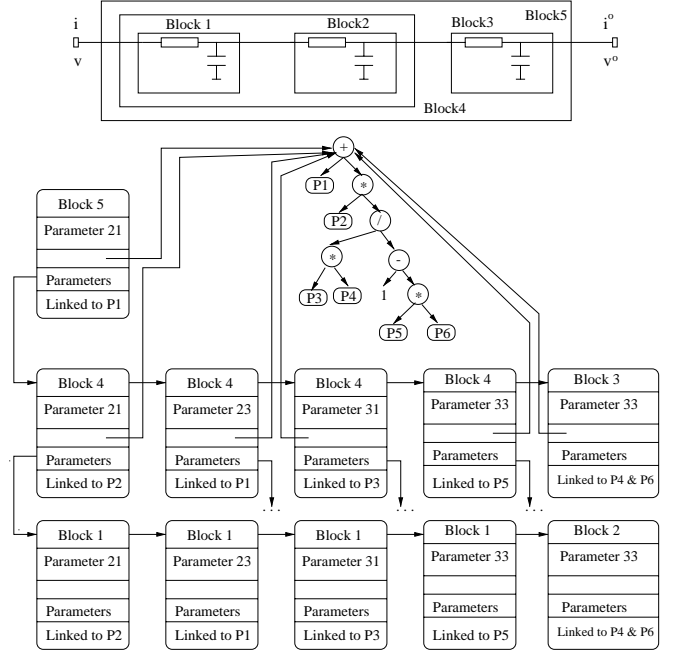


Figure 5: DSN Performance Model for power bus

Parameters  $a_{i,j}^{res}$  correspond to the composed block. These formulas permit calculating the parameters  $DPB^{l,j}$  and  $APB^{l,j}$ .

To complete the power net model, the model for the contact to the power net must be provided (Figure 2). Similar to [1] and [7], contacts are modeled as an inductance with a value of 10nH in series with a resistance of 100mΩ. Thus, matrix  $C^{l,j}$  (Figure 2) is a constant matrix.

## 2.3 Representation of DSN Models

Formulas for substrate, power bus and contact parameters are used to build symbolic performance models (PM) for DSN evaluation. If current variations due to digital switching are known (from the noise signature of a block) then voltage variations at power pins of analog blocks can be computed using PMs. Because of space limitations, we detail next symbolic PMs for power buses, only. However, similar PMs are set-up for substrate, contacts and entire noise propagation paths.

Top part of Figure 5 shows a power bus consisting of three segments. Segments are represented as *Block 1*, *Block 2* and *Block 3* and their parameters are similar to those of the matrix in Figure 4(a). *Block 4* and *Block 5* are composed blocks described by Figures 4(b) and (c). Their parameters are similar to parameters  $a_{i,j}^{res}$  shown in the previous subsection.

Bottom part of Figure 5 depicts a fragment of the symbolic PM that relates parameter  $a_{21}$  of *Block 5*. This parameter is used to calculate the influence of current  $i$  on voltage  $v^o$ . PM contains meta-nodes that indicate what

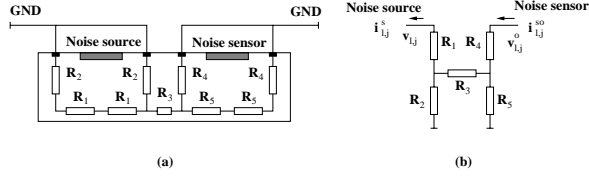


Figure 3: **Resistive macro-model for substrate coupling**

matrix  $C^{l,j}$ , digital power bus by matrix  $DPB^{l,j}$  and analog power bus by matrix  $APB^{l,j}$ . First, we applied Kirchoff's laws and definitions of matrices of the two-port blocks. Formulas to relate parameters  $TRR_{m,n}^{l,j}$  to the parameters of substrate, power nets and contacts were obtained by solving this equation set. Due to space limitations, we do not provide the resulting formulas. Following subsections detail how matrices  $S^{l,j}$ ,  $C^{l,j}$ ,  $DPB^{l,j}$  and  $APB^{l,j}$  relate to the physical and geometrical characteristics of substrates, contacts and power buses.

## 2.1 Coupling through substrate

Coupling through substrate is due to the finite resistivity of substrate and junction capacitances. As a result, a current pulse flows between a switching digital node and surrounding substrate, and produces a voltage variation at the supply pins of an analog circuit. Verghese *et al* [9] and Ku *et al* [5] present resistive and capacitive models for substrate. As application bandwidth is less than 1 GHz, in this paper we adopted the resistive substrate modeling proposed by Joardar [4]. Model consists of a net of resistances as shown in Figure 3(a). Expressions for resistances are derived depending on their geometrical dimensions [4]. If resistive substrate model is not sufficient then mesh model [7] [9] for substrate can be employed without invalidating the proposed transient analysis method.

Coefficients  $S_{m,n}^{l,j}$  result by writing Kirchoff's current and voltage laws for the circuit in Figure 3(b) and expressing unknown voltages  $v_{l,j}$  and  $v_{l,j}^o$  depending on currents  $i_{l,j}^s$  and  $i_{l,j}^o$ . Following formulas resulted:

$$S_{11}^{l,j} = -(R_1 + \frac{2R_2R_3}{R_2+2R_3}) \quad S_{12}^{l,j} = \frac{R_2R_3}{R_2+2R_3}$$

$$S_{21}^{l,j} = -\frac{R_2R_5}{R_2+2R_3} \quad S_{22}^{l,j} = (R_4 + \frac{(R_2+R_3)R_5}{R_2+2R_3})$$

## 2.2 Coupling through power supply lines

Stanisic *et al* [7] indicate that power buses can be modeled as a set of RC segments. Relationships that express resistance and capacitance of a segment depending on segment length, height and width are presented in [7]. For transient analysis, influence of state variables  $Q_k^{l,j}(t)$  (charges stored by segment capacitances) needs to be captured. To find coefficients

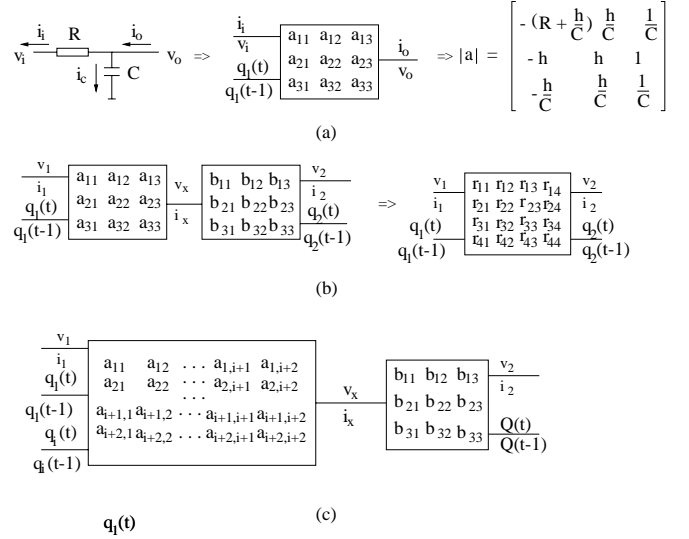


Figure 4: **Transient analysis of a power bus**

$DPB_{m,n}^{l,i}$  of the power bus of digital block  $i$  and coefficients  $APB_{m,n}^{l,j}$  of the power bus of analog block  $j$ , relationships between known currents at the two ends of a segment, charges stored by capacitances and unknown voltages need to be established. We refer to Figure 4(a) for this task.

Transient analysis of an RC segment results by solving the following set of differential and algebraic equations (DAEs) (equations represent Kirchoff's and Ohm's laws and definition of capacitance):

$$\dot{q}(t) = ic(t) \quad i_o(t) = i_c(t) + i_i(t)$$

$$i_i(t) R = v_o(t) - v_i(t) \quad v_o(t) = \frac{q(t)}{C}$$

Charge value  $q(t-1)$  stored by capacitor  $C$  at previous time moment is known. Besides the two voltages, charge  $q(t)$  at the current time moment is also unknown.

Previous set of DAEs cannot be directly solved with an analytical method because of the derivative of charge  $q(t)$ . Instead, derivate  $\dot{q}(t)$  can be replaced by the Backward Euler integration formula [7]  $\dot{q}(t) = \frac{q(t) - q(t-1)}{h}$ . Constant  $h$  is the integration step. After replacing  $\dot{q}(t)$  and solving the resulting equation set, we obtained following formulas for unknowns  $q(t)$ ,  $v_i(t)$  and  $v_o(t)$ :

$$v_o(t) = \frac{1}{C}(q(t-1) + h(i_o(t) - i_i(t)))$$

$$v_i(t) = \frac{1}{C}(q(t-1) + h(i_o(t) - (RC + h)i_i(t)))$$

$$q(t) = q(t-1) + h(i_o(t) - i_i(t))$$

Hence, for transient analysis, the RC stage can be modeled as a three-port block, where two ports describe the physical ports of the stage (these ports are described by a pair current-voltage) and a virtual port that has as a known the charge value  $q(t-1)$  and as an unknown the charge value  $q(t)$  (Figure 4(a)). Figure 4(a) also depicts the symbolic matrix that characterizes the three-port representation of an RC stage.

To complete power net modeling, a composition rule is

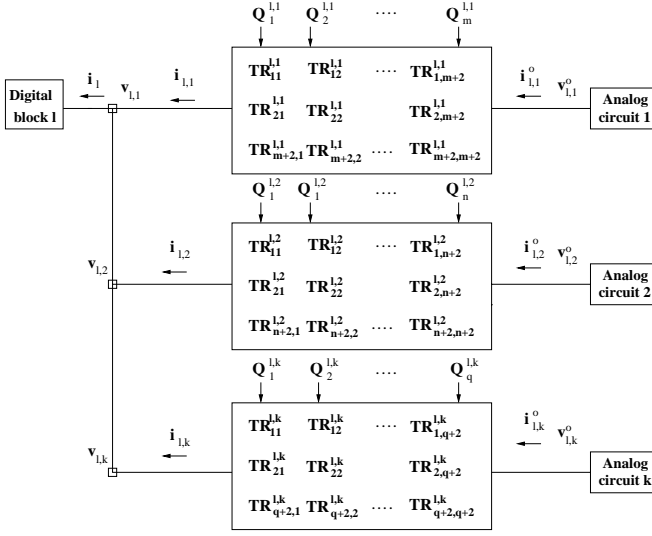


Figure 1: Model for single DSN source

lated by the superposition principle [1]. A current spike  $i_l$  that originates at the power supply of digital block  $l$  determines a voltage variation  $v_{l,t}^o$  at power supply of analog block  $t$ . Voltage variation due to all digital circuits at power supply of analog block  $t$  is

$$v_t^o = \sum_{i=1}^p v_{i,t}^o$$

Thus, DSN that is due to each digital circuit and propagates at the power pins of an analog block has to be calculated.

Figure 1 presents the model for transient analysis. The model includes a digital noise source (digital block  $l$ ) and noise distribution paths to each of the  $k$  analog blocks. Analog and digital power buses are separated in this model. This is a valid assumption for most cases as current design practice separates analog and digital power lines [1] [7]. If power lines are shared (for reducing number of I/O pins) then same reasoning can be applied to evaluate noise. Current  $i_l(t)$  is due to the switching of block  $l$  and is characterized by the signature of digital block  $l$ . Currents  $i_{l,1}^o(t), i_{l,2}^o(t), \dots, i_{l,k}^o(t)$  are also known and depend on the impedances of the analog blocks (for our case we assumed these currents to be zero). Voltages  $v_{l,1}^o(t), v_{l,2}^o(t), \dots, v_{l,k}^o(t)$  represent DSN as they are voltage variations due to the current  $i_l$ . Symbols  $TR_{i,j}^{l,m}$  are matrix coefficients of the two-port representations of DSN propagation paths. Influence of state variables i.e. the charges  $Q_p^{l,i}(t-1)$  stored by capacitors has to be captured by the equation set. Calculating charge values is presented in more detail when discussing modeling of power supply buses (Sub-

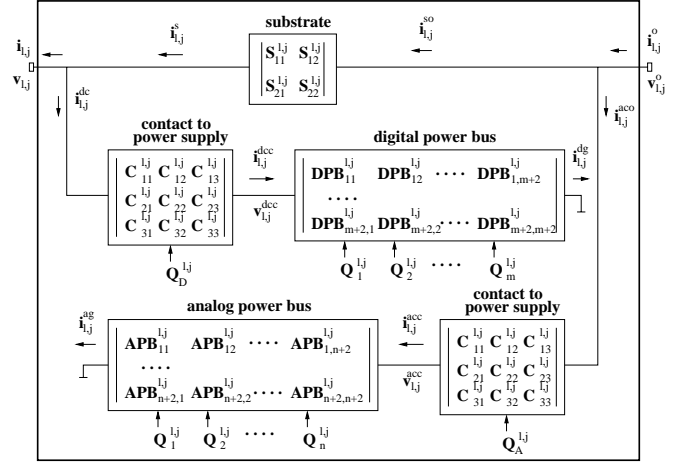


Figure 2: Noise path modeling

section 2.2).

Using Kirchoff's laws and definitions of matrices  $TR_{i,j}^{l,m}$ ,  $m = 1$  to  $k$ , following equation was set up:

$$\begin{aligned} i_l(t) &= i_{l,1}(t) + i_{l,2}(t) + i_{l,3}(t) + \dots + i_{l,k}(t) \\ v_{l,1}(t) &= v_{l,2}(t) = \dots = v_{l,k}(t) \\ v_{l,1}(t) &= TR_{11}^{l,1} i_{l,1}(t) + TR_{12}^{l,1} i_{l,2}(t) + \sum_{p=1}^m TR_{1,p+2}^{l,1} Q_p^{l,1}(t-1) \\ v_{l,1}^o(t) &= TR_{21}^{l,1} i_{l,1}(t) + TR_{22}^{l,1} i_{l,2}(t) + \sum_{p=1}^m TR_{2,p+2}^{l,1} Q_p^{l,1}(t-1) \\ v_{l,2}(t) &= TR_{11}^{l,2} i_{l,1}(t) + TR_{12}^{l,2} i_{l,2}(t) + \sum_{p=1}^n TR_{1,p+2}^{l,2} Q_p^{l,2}(t-1) \\ v_{l,2}^o(t) &= TR_{21}^{l,2} i_{l,1}(t) + TR_{22}^{l,2} i_{l,2}(t) + \sum_{p=1}^n TR_{2,p+2}^{l,2} Q_p^{l,2}(t-1) \\ &\dots \\ v_{l,k}(t) &= TR_{11}^{l,k} i_{l,1}(t) + TR_{12}^{l,k} i_{l,2}(t) + \sum_{p=1}^q TR_{1,p+2}^{l,k} Q_p^{l,k}(t-1) \\ v_{l,k}^o(t) &= TR_{21}^{l,k} i_{l,1}(t) + TR_{22}^{l,k} i_{l,2}(t) + \sum_{p=1}^q TR_{2,p+2}^{l,k} Q_p^{l,k}(t-1) \end{aligned}$$

Formulas for unknown voltages  $v_{l,1}^o(t), v_{l,2}^o(t), \dots, v_{l,k}^o(t)$  result by solving this equation set. For analog block  $i$ , voltage variation at its power supply line is given by

$$v_{l,i}^o(t) = \frac{TR_{21}^{l,i}}{TR_{11}^{l,i}} \left( \frac{i_l(t) + \sum_{j=1}^k \frac{\sum_p TR_{1,p+2}^{l,j} Q_p^{l,j}(t-1)}{TR_{11}^{l,j}}}{\sum_{j=1}^k \frac{1}{TR_{11}^{l,j}}} \right) - \sum_p TR_{1,p+2}^{l,i} Q_p^{l,i}(t-1) + \sum_p TR_{2,p+2}^{l,i} Q_p^{l,i}(t-1)$$

Finally, overall voltage variation at power supply line of analog block  $i$  is computed by summing voltages  $v_{l,i}^o$  due to all digital blocks.

Symbols  $TR_{m,n}^{l,j}$  describing each noise propagation path  $j$  were calculated for completing DSN modeling. Figure 2 presents the noise propagation path between digital circuit  $l$  and analog block  $j$ . The figure was used to motivate how coefficients  $TR_{m,n}^{l,j}$  relate to the coefficients that characterize the substrate, contacts and analog and digital power buses. Coefficients assume that currents  $i_{l,j}$  and  $i_{i,j}^o$  are knowns and voltages  $v_{l,j}$  and  $v_{i,j}^o$  are unknowns. Let's assume that substrate is described by matrix  $S^{l,j}$ , contact to power supply by

# Fast Evaluation of Digital Switching Noise for Synthesis of Mixed-Signal Applications

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## Abstract

*This paper presents a novel symbolic analysis method for transient analysis of digital switching noise (DSN). The method relies on symbolic techniques to express the voltage variations at the power pins of analog blocks depending on the DSN at the switching digital blocks. The paper discusses the modeling of DSN propagation including the representation of the substrate coupling, contacts to the power supplies and power buses. Our experiments support the correctness of the method, and showed significant speed-ups of simulation time as related to SPICE simulation.*

## 1 Introduction

Single chip integration of analog and digital hardware offers critical advantages such as cost reduction and yield enhancement with an improvement in high-frequency performance. Design of mixed-signal chips with existing analog and digital synthesis tools is not satisfactory in most of the cases. There is a very high chance that performances of the separately synthesized digital hardware do not match design requirements of analog circuits. For example, encouraging operation concurrency for satisfying throughput constraints might result in a high digital switching noise (DSN), that perturbs a correct functioning of analog blocks. Hence, for mixed-signal applications, digital high-level synthesis (HLS) must contemplate not only traditional performances (such as area, speed, power) but also constraints imposed by analog circuits.

For a mixed-signal system, noise is not only the major design concern but also the most specific one [1] [2] [7] [9]. Noise sources are located in both the analog and digital domains. Analog noise is produced by analog circuits themselves and is due to physical properties (such as random movement of charges, charge re-combinations, etc.) of the semiconductor material that devices are built of. However, mixed-signal design experience motivates that digital switching noise (DSN) is both the biggest noise source and the most

restrictive design constraint in a mixed-signal IC [1] [7] [9]. DSN is generated by the switching of digital components. The amount of noise that can be accommodated at the power pins of an analog block is characterized by its *Power Supply Rejection Ratio* (PSRR) [3]. A high DSN can compromise the correct functioning of analog circuits. Moreover, analog circuits with a high PSRR are difficult to design and require more area [1]. Therefore, digital hardware has to be designed so that its DSN is less than the limits acceptable to analog circuits.

This paper presents original technique for DSN evaluation. This modeling is crucial for verifying the correct functioning of the overall mixed-signal implementation that was synthesized. *Symbolic* models are automatically derived for noise propagation paths. If current variations due to digital switchings are known then transient voltage variations at the power pins of analog blocks can be computed using these symbolic models. We are not aware of any other DSN evaluation technique for HLS. Experiments showed that symbolic models permit DSN evaluation with the same accuracy as SPICE simulation in a significant shorter time. Short evaluation time is critical for analyzing the many design alternatives generated by HLS.

The paper is organized as four sections. Section 2 explains the suggested technique for DSN evaluation. Section 3 presents experimental results for studying the effectiveness of the proposed approach. Finally, we provide our conclusions.

## 2 DSN Evaluation

The two major noise-propagation paths in a mixed-signal IC are (1) coupling through substrate and (2) coupling through power supply lines [7]. Coupling between interconnections (crosstalk) is small as compared to other two coupling types, if analog and digital hardware are separated at the floorplan level [1]. If digital domain contains  $p$  digital circuits then total noise that appears at an analog block can be calcu-