

Using standard analog HDLs for compact modeling

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Mainstream device models

- **Used by many 10,000 designers**
- **It pays to invest in optimizing the code for efficiency**
 - **Need access into simulator to tune for numerical stability and convergence**
- **“Not quite ready for prime time” is not good enough**
 - **Not suitable for “casual” modelers**
- **C will continue to be the modeling language**

Niche device models

- **Used by small clientele**
- **Difficult to justify the investment to optimize the code for efficiency, or tune for numerical stability and convergence**
- **“Not quite ready for prime time” may be acceptable**
- **Standard HDLs may be advantageous**

Standard analog HDLs and compact models

- **No mainstream compact models today are coded in standard analog HDLs**
- **But there are reports of some such activities**
 - **May improve modeling productivity**
 - **Appealing for “casual” modelers**

Standard analog HDLs

- **Verilog-AMS & VHDL-AMS lack some functionalities for compact modeling**
- **Coding compact models was not a prime design objective of analog HDLs**
- **Typically, analog HDLs were designed for**
 - **Top-down design flow**
 - **Multi-level simulation**
 - **IP re-use**

Standard analog HDLs (cont.)

- **Learning curve issue: today's device modelers or programmers lack expertise in Verilog-AMS or VHDL-AMS**
 - **Takes time to change**
- **Technical issue: need access into simulator to tune for numerical stability and convergence**
 - **Language, software and expertise**