

VHDL-AMS implementation

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ARCHITECTURE behav OF system IS
    PORT (n1,n2,n3,n4: ELECTRICAL;
          t1,t2: THERMAL);
BEGIN
    -- resistor (behav)
    C MAP (2.0)
    AP (n1,electrical_ground);
    -- th_resistor (behav)
    C MAP (10.0,0.1)
    AP (n2,electrical_ground,t1);
    ...
END behav;
```

```
ENTITY material IS
    GENERIC (Ta: REAL);
    PORT (TERMINAL t1,t2: THERMAL);
END;
```

```
ARCHITECTURE behav OF material IS
    QUANTITY t_1 ACROSS h_1 THROUGH t1 TO thermal_1;
    QUANTITY t_2 ACROSS h_2 THROUGH t2 TO thermal_2;
    CONSTANT k : REAL := 1.412;
    .....
    CONSTANT dy : REAL := Height/(M-1.0);
    QUANTITY PkA1, PkA2: REAL;
    QUANTITY T11, T12, ... T104, T105:REAL;
BEGIN
    BREAK T11 => Ta;
END;
```

Subst
mate