

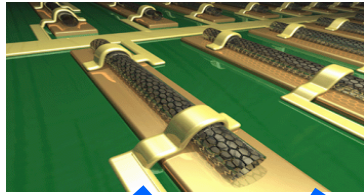
What is the real impact of Behavioral Modeling and Simulation on IC Design

J. White

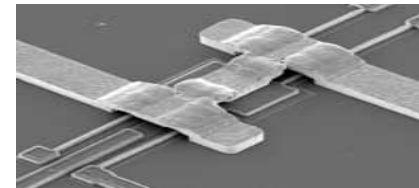
BMAS04 Panel

MegaCycle Simulation Problem

CNT
FET

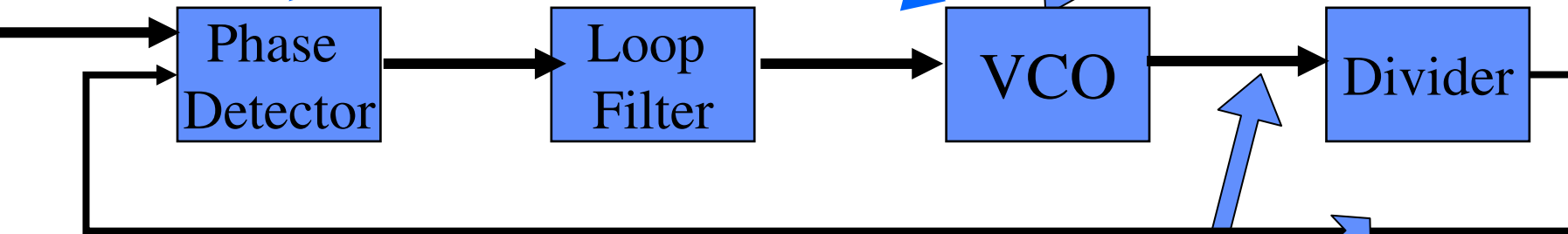


Bachtold, et al.,
Science, Nov. 2001

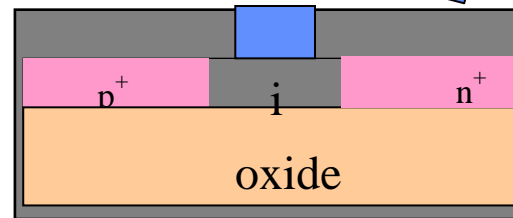


Micromachined
Resonator

www.discera.com



Kimerling
Group



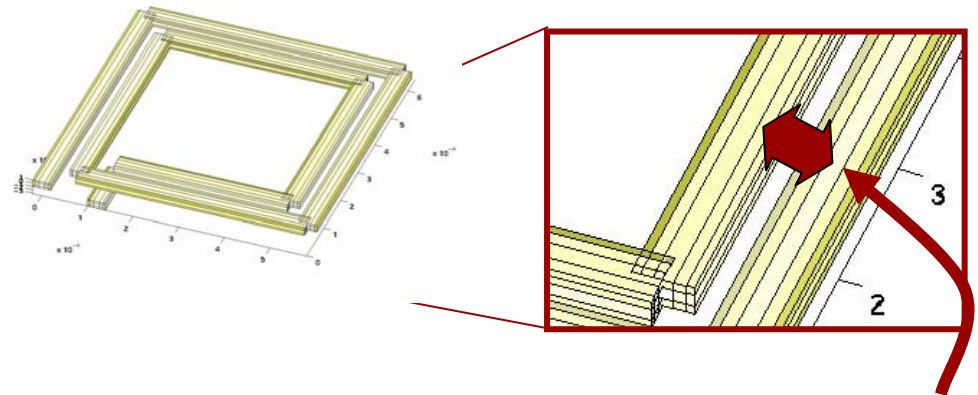
Opto-electrical
transducers

Megacycle Simulation Needs Reduced-Order Models – PLL Capture, Eye Diagrams, A-D distortion

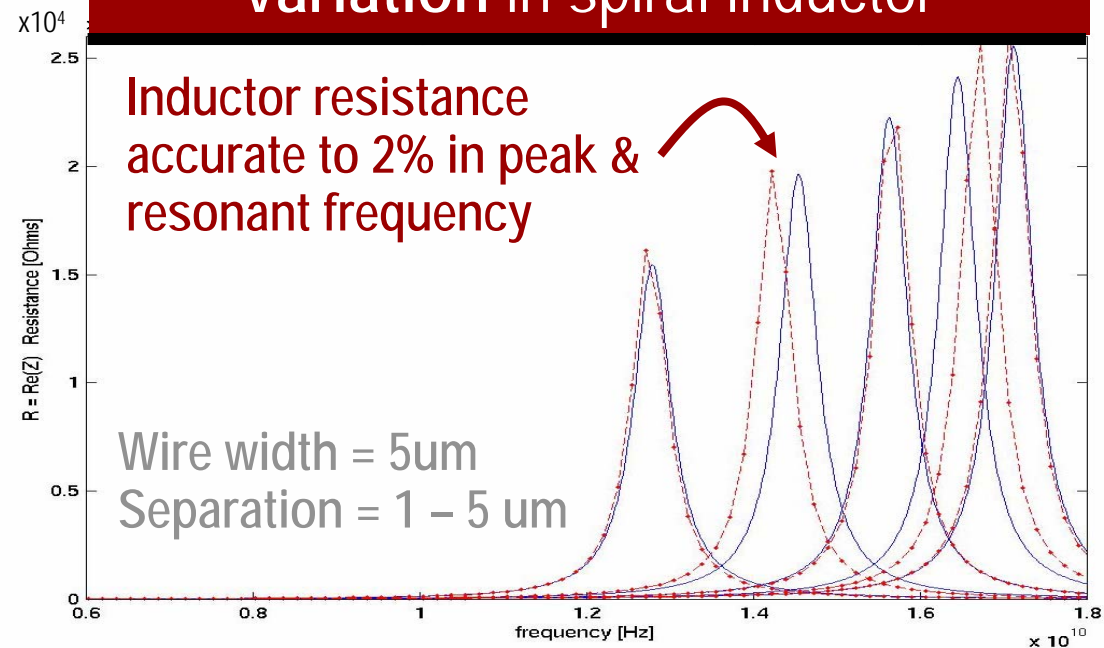
- Automatic cell (subcircuit) reduction for faster simulation
 - Automatic or its NOT VERIFICATION!

Accurate Parameterized Models for Yield Analysis and Design Optimization

- Extract parameterized models from 3-D sim's
 - Allows arbitrary geometry (e.g. rectangular or hex spiral L's)
 - Parameterized models 100→1000x faster to evaluate
 - **Supports hierarchical optimization**
- ...and if model construction is fast enough
 - Can account for surrounding interconnect already laid out



Parameterized model for spacing variation in spiral inductor



What is the future of Model Compilers (Slide thanks to J. White, Ansoft Corporation)

- **Simulation Companies are differentiating on ability to work with Behavioral models**
 - Is there a behavioral model flow efficient enough for compact models?
 - Include big digital, IBIS, etc?
 - Will they need the compiler in house?
 - Maybe they have custom helpful simulator directives?
 - Device collapsing (new netlist?), topology opts, by-pass, linearity, etc?
 - Incremental Compilation (S->rational, etc)
- **Will there be a role for compiler companies?**
 - Will too coupled to a simulator company?
 - What about public domain model compilers?
 - Will model debugging tools secure their role?