

Modeling remote system for sensor monitoring using Verilog HDL and SIMULINK® co-simulation

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ABSTRACT

The aim of this study is to model and design an efficient wireless system that should be easy to integrate with other technologies or infrastructures at a low cost. The system is reading analog information recorded by a biomedical sensor in a transmitting unit attached to the patient. The recorded data is converted digitally using ADC and sent to FSK transmitter through FPGA. Verilog HDL has been used to implement the required functions of the FPGA. SIMULINK® software has been used to model and simulate Frequency-Shift Keying (FSK) Transmitter/ Receiver suitable for short-range communications. A two-tone FSK signal is generated, passed through a noisy channel, down converted to baseband and passed to FM detector to restore the original transmitted bit stream. The behavioral HDL design has been interfaced to the SIMULINK model and the overall performance has been verified.

1. INTRODUCTION

Home health care costs have increased by 400% in the last 5 Year. Although increased hospital or nursing home care can be delivered in the patient's home, professional services such as clinical and medication monitoring are still required.

On the other hand, advances in wireless and Internet technology are developing rapidly have opened new opportunities for the health services to reconsider the traditional model of patient care [1]. In the next 25 years, the global population over the age of 65 will increase by 88% [2].

The challenge is to raise or at least maintain the present level of health care provision without ending up in an uncontrolled cost explosion. An increasing number of researchers and manufacturers are working to develop a new generation of wireless technology applications for the medical field to improve the quality and to reduce the cost of patient care [3]

One of the areas in healthcare that best lend itself to wireless technology is patient monitoring, also known as wireless telemetry. By attaching a wireless monitoring device to the patient's bedside or directly to the patient, physicians can monitor vital signs from down the hall or across town.

The most critical features of wearable health monitoring equipment are long battery life, lightweight, and small dimensions [4]. Continuous monitoring during normal activity also requires that the device can be hidden to protect user's privacy. In order to make the monitoring devices easily wearable and suitable for the patient, they need to be designed ergonomically [5]. The equipment must also produce high-quality signals, be easy to apply and remove, be robust and suitable for different environments and users, both male and female [5].

The aim of this work is to present a useful model that combines both hardware and software environments and achieves the described demands. The key features of the introduced models are the low complexity, low power consumption and efficient data transmission.

2. SYSTEM SPECIFICATIONS

The main blocks of the system are sketched in Fig 1. First an 8-bits ADC will handle the analog signal recorded by the sensor readout circuit.

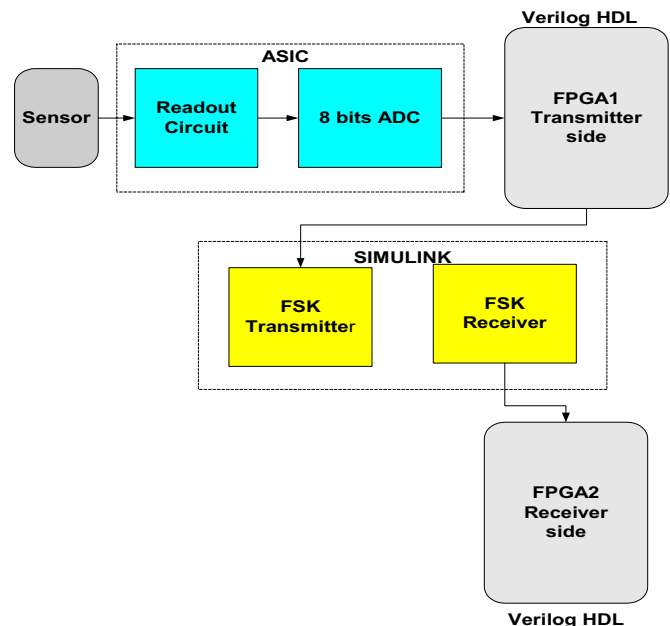


Figure.1. Block diagram of the system

The FPGA then makes the different processing on the coming digital data like buffering, compression and framing, and then send the data to the FSK transmitter model.

Behavioural models for both transmitter/receiver have been implemented on SIMULINK based on the Direct-conversion architecture [6]. A novel logic detector has been modelled at the receiver side to recover the transmitted symbols. A second FPGA is interfaced to the output of the receiver and responsible for processing the data inversely like de-framing and de-compressing. A detailed description of the HDL model will be presented in the following section. Active-HDL[®] interface has been used to invoke the HDL modules in the Matlab and SIMULINK environment

3. FPGA DESCRIPTION

FPGAs are based on flexible regular structures, which upon configuration can emulate both sequential and combinational logic circuits. These flexible structures contain four major types of blocks: the logic block (LB), the interconnect structure, the connection block (CB) and the input/output block (I/O).

The main blocks of the transmitter side FPGA are shown in Fig.2. The different units of the system were coded with verilog HDL using ModelSim V6.0 and synthesized using XILINX ISE7.1. The final implementation was targeting Virtex Pro device since it provides various features that solve designer's challenge throughout the system.

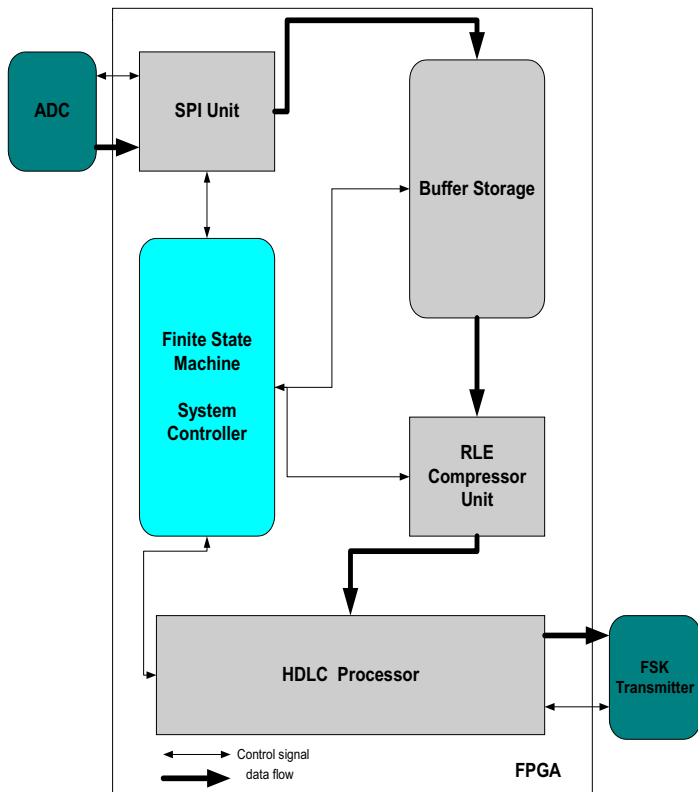


Figure.2. Building blocks of the transmitter FPGA

From the figure above, the FPGA consists mainly from an SPI (Serial Peripheral Interface), RLE (Run Length Encoding) compressor and HDLC (High Data Link Control) compressor units. The operation of the system units and the flow of data through the system are controlled by a main FSM (Finite State Machine) controller. Both compressor and framer will be discussed in the following two sections.

3.1. RLE Compressor

Data compression will be effective when the measured signals are expected to be slow and repeatable. The task of this unit is then crucial to the system power performance. Run Length Encoding is a conceptually simple form of compression. RLE consists of the process of searching for repeated runs of a single symbol in an input stream, and replacing them by a single instance of the symbol and a run count. A simple flow chart of the RLE implementation is shown in Fig.3.

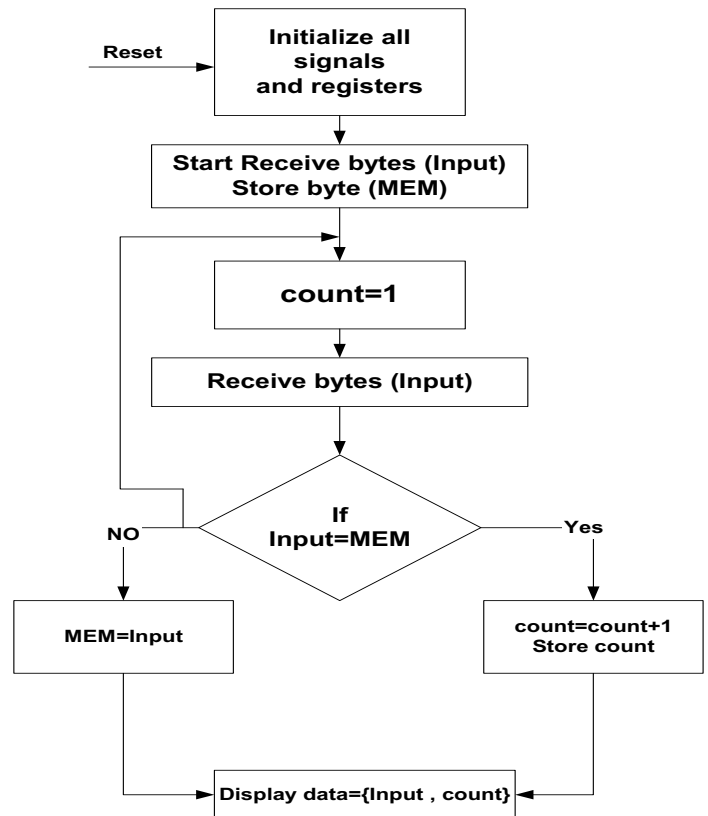


Figure.3. RLE compressor implementation

A sample of the output simulation waveforms is shown in Fig.4. Three waveforms have been marked, these are the input data bytes, valid data signal which is active (high) when there is a new or not repeated data and the two bytes (input and count) output data.

The HDL code for the compressor has been written as a state machine and optimized to only two states. The code also has been synthesized successfully to achieve good

device utilization. It is worth to mention that other types of compression techniques have been considered in this work, but it was found that with RLE is more suitable in terms of design complexity, power resources and compression performance.

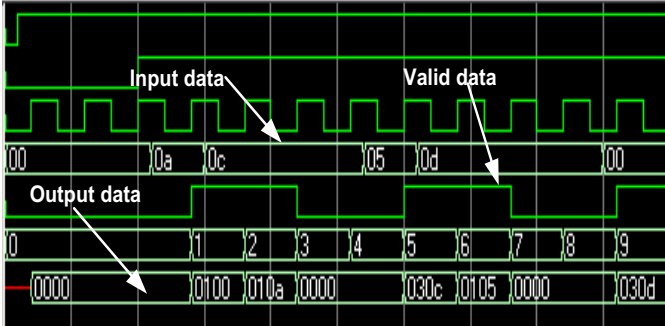


Figure.4. Simulation output waveforms of RLE compressor

4. HDLC FRAMER

This unit is considered to be the main core of the system model where the data are grouped into frames and sent to the transmitter. HDLC protocol is a bit oriented protocol that is used as a data link of most of current communication systems [7]. The main features provided by this protocol are:

- Synchronous operation
- Start and end of frame pattern generation
- Zero insertion and removal for transparent transmission
- Cyclic Redundancy Check (CRC) generation for error handling

4.1 HDLC frame

The basic structure of the HDLC frame is shown in Fig.5

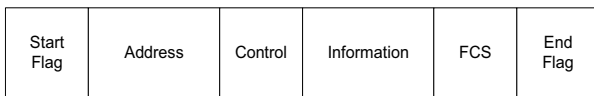


Figure.5. Main fields of the HDLC frame structure

- Start and end flags, represented by the sequence (01111110), are required for synchronous transmission.
- Address field is used to identify the destination address at the receiver side
- Control field is used to classify the HDLC frames according to the link configuration type.
- Information field contains the transported data
- FCS (Frame Check Sum) is used to detect errors by adopting CRC generation

4.2 System implementation

The main blocks of HDLC transmitter are shown in Fig.6. A finite state machine (FSM) is responsible for generating

all the necessary internal control signals required by the different modules.

First, the controller checks if there is a valid data output from the compressor and then it will start loading the bytes into FIFO memory storage. Then the data will be read serially from the memory storage and sent to the CRC module to generate the frame check sequence (FCS).

The bit stuffer is responsible for examining the frame content and checking every 5 consecutive 1's bits including FCS bits. If 5 consecutive 1's are detected, a 0 bit is inserted into the serial bit stream. This will help the receiver to distinguish the actual data transmitted. The start and end flags are generated at the final stage and attached to the frame. Also the transmitter will fill the gaps between the frames when the transmission is idle by sending a sequence of 8consecutive 1's

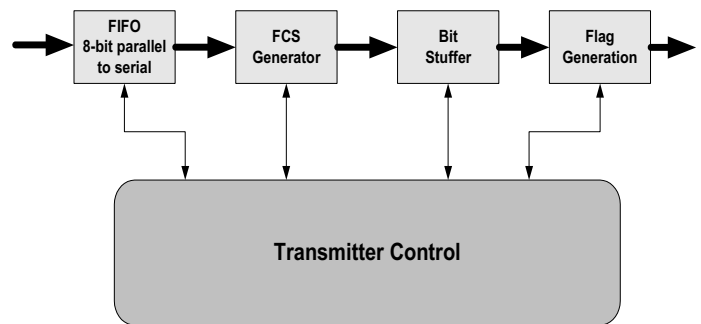


Figure.6. HDLC transmitter control block diagram

The received frames are processed inversely by similar structure at the receiver control to recover the transmitted bytes. All the modules of both HDLC transmitter and receiver have been modelled, simulated and synthesized successfully.

5. FSK TRANSMITTER/RECEIVER SIMULINK IMPLEMENTATION

A detailed description of the simulated FSK transceiver model is given in this section

5.1 FSK transmitter model

In Fig.7, a simple FSK modulator is simulated and implemented using SIMULINK® as shown in Fig.2.

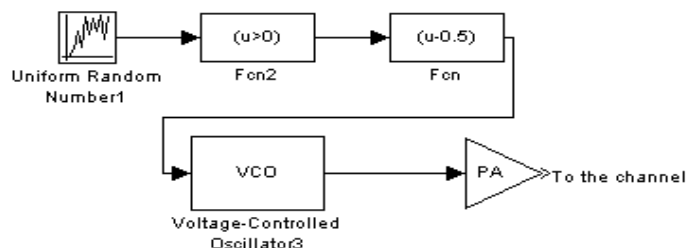


Figure. 7. Modeling FSK transmitter

A uniform random number generator is employed to output a random bit stream of 0 and 1's with a specific data rate. The input voltage to the Voltage Controlled Oscillator (VCO) is shifted either to ± 0.5 instead of 0 or 1. This is implemented in order to get an equal frequency shift for the both tones by multiplying this input value by the sensitivity of the VCO.

The power amplifier (PA) is modeled to be a non-linear unit since it exhibits a higher efficiency of 60% for some of the power efficient modulation techniques as the FSK [6]. This can be explained, as the FSK waveforms have no abrupt phase change and exhibit a constant envelope. Therefore the FSK signals can therefore be amplified by means of nonlinear PAs with no spectral regrowth

5.2 FSK Receiver model

Direct-conversion *homodyne* receiver is modeled as shown in Fig.8. The low-noise amplifier (LNA) represents the first gain stage in the receiver path and its noise figure is added directly to that of the system. A small signal non-linearity, compression, saturation, slew rate limiting, and two types of noise (white and flicker) are modeled within the (LNA) unit as shown in Fig.9.

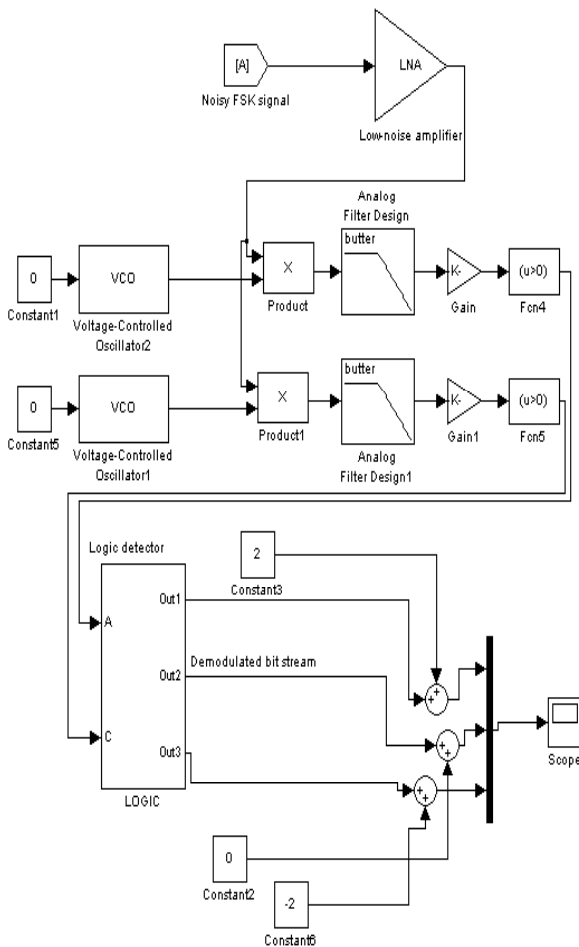


Figure. 8. Modeling FSK direct-conversion receiver

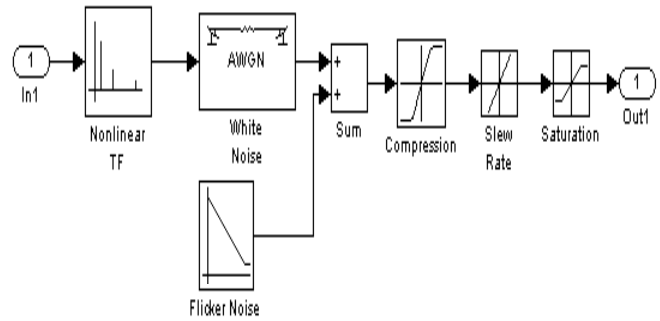


Figure. 9. Modeling a non-linear LNA unit

5.3 Symbol (logic) detector

The design of this block has a crucial effect on the system overall performance and its design needs to be fully understood. The main function of the unit is to recover properly the bit symbols of the input signal using a logic system. The details of this unit in SIMULINK® are shown in Fig.10.

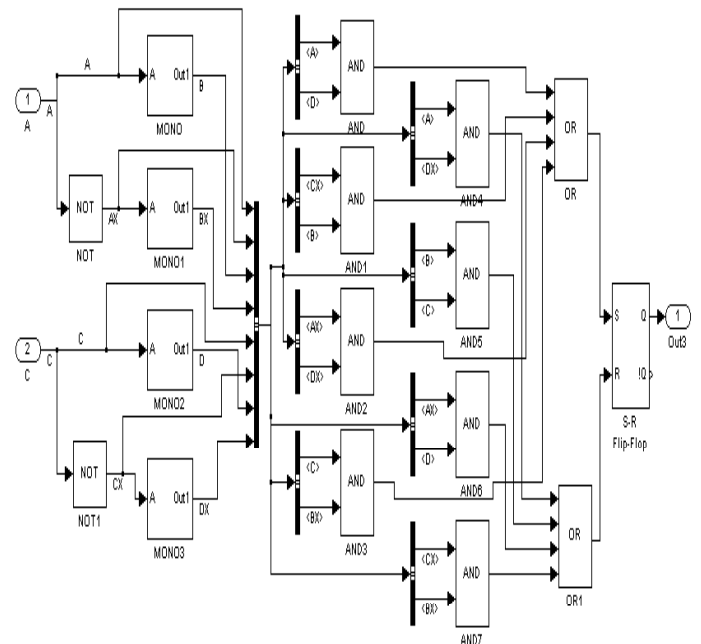


Figure. 10. Modeling symbol logic detector

Combinational logic units used to process the incoming signals from the two-quadrature channels. The output bit value is extracted at the final stage by a S-R flip-flop.

5.4 Modeling Channel propagation effects

The channel model is a representation of the input-output relationship of the channel in mathematical or algorithmic form. Developing the mathematical models for the propagation of the signals over a noisy transmission medium requires a good understanding of the underlying physical phenomena. One of the challenges in channel

modeling is the translation of the detailed physical propagation into a form that is suitable for simulation. The SIMULINK[®] is a powerful tool that has huge advantages in being able to build realistic mathematical models. In Fig. 11, a propagation channel model for a single path FSK signal with two effects, adding Additive White Gaussian noise (AWGN) and short distance (0.5 m) path loss, is presented.

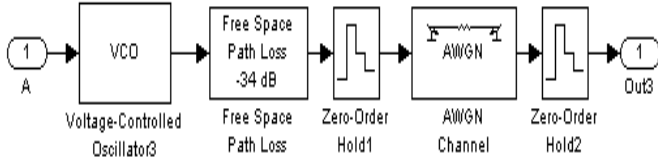


Figure. 11. Modeling channel with White noise and path loss

A) *Inband and Outband Interference model*

A major limiting factor in the performance of wireless RF systems is the interference. Sources of interferences include another transmitter device operating either in the same frequency or neighboring frequency bands. The two major types of system-generated interference are co-channel (in band) and adjacent (outband) channel interference. Inband channel interference is defined as undesired signals with frequency components that fall within the receiver’s RF passband. On other hand, outband channel interference is defined as signals with frequency components that are significantly removed from the receiver’s RF passband. In SIMULINK[®], a simple model for system interference can be constructed by combining the output signals from a number of different FSK transmitters as shown in Fig. 12.

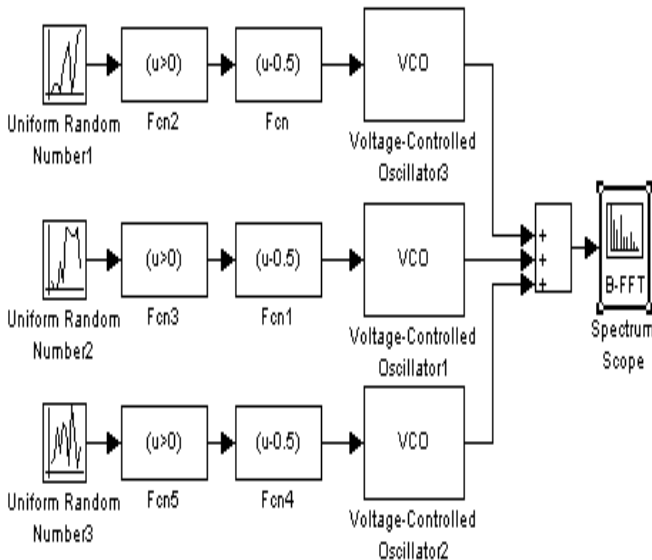


Figure.12 Modeling the system interference

From the figure, VCO2 and VCO3 output FSK signals with inband and outband frequencies with respect to the transmission band of VCO1.

B. *Rayleigh Multipath Fading model*

Rayleigh distribution is commonly used to describe time varying nature of the received envelope of a flat fading signal. Fig. 13 shows a SIMULINK[®] implementation of a three-rays Rayleigh fading model.

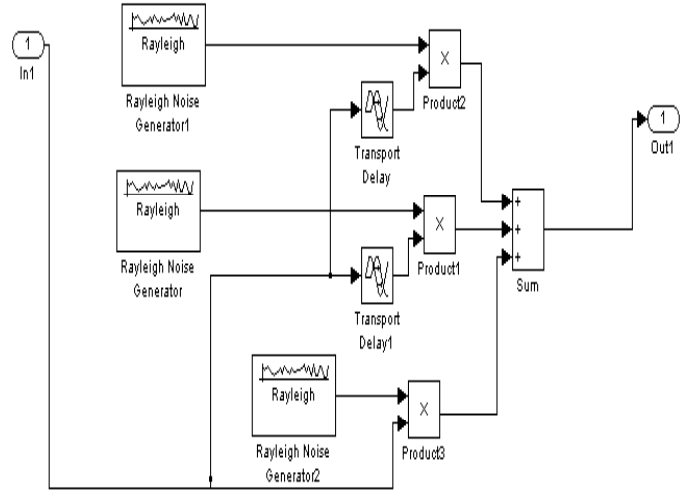


Figure.13 Modeling of multipath Rayleigh fading channel

Rayleigh generator unit is based on the rule that summing two quadrature Gaussian noise signals obeys a Rayleigh distribution. The probability distribution function (pdf) of Raleigh distribution is given by the following equation:

$$p(r) = \begin{cases} \frac{r}{\sigma^2} \exp\left(-\frac{r^2}{2\sigma^2}\right) & 0 \leq r \leq \infty \\ 0 & r < 0 \end{cases} \quad (1)$$

where σ is the r.m.s value and σ^2 is the time average-power of the received signal before detection. The mean value r_{mean} of the Rayleigh distribution is given by:

$$r_{mean} = E(r) = \int_0^{\infty} r p(r) dr = 1.2533\sigma \quad (2)$$

The variance of rayleigh distribution is given by σ_r^2 , which represents the ac power in signal envelop as follows:

$$\sigma_r^2 = E[r^2] - E^2[r] = \int_0^{\infty} r^2 p(r) dr - \frac{\sigma^2 \pi}{2} = 0.4292\sigma^2 \quad (3)$$

The median value or r is found by solving:

$$\frac{1}{2} = \int_0^{r_{median}} p(r) dr \Rightarrow r_{median} = 1.177\sigma \quad (4)$$

Thus the mean and the median should differ only by 0.55 dB in Raleigh fading signal.

The time delay units represent the multipath delay time spreads and they typically take values up to 100ns for outdoor propagation and between 30-60 ns for indoor propagation [8].

7. CONCLUSIONS

In this paper, a mixed hardware and software simulation environments have been used to model a remote short-range wireless system. Although HDL provides many high level abstractions and language constructs for behavioral modeling, its synthesizable subset is far too restrictive for system level design.

On the other hand, SIMULINK environment provides powerful high-level mathematical modeling environment for digital communication systems that can be widely used for algorithm development and verification.

The main two operations implemented by the transmitter FPGA are compression and framing. RLE has been used to compress the stored data bytes efficiently with an optimal number of states. The HDLC protocol has been used successfully for framing the data and providing error-handling mechanism to the receiver. All the FPGA modules have been verified and implemented using XILINX Virtex 2 pro device. During the development of the verilog codes, it our main goal was to make all the units synthesizable.

An FSK transmitter suitable for short-range wireless communications has been implemented in SIMULINK. A detailed description for both transmitter and receiver units was given. Different channel propagation effects like noise, path loss, multipath fading, and interference were introduced in the model. The transceiver system performance was tested under different conditions. The implemented model showed a good capability in recovering the original data at the receiver side with different transmission frequencies. The simulation running time is considered to be the main limitation of using SIMULINK.

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