

VHDL-AMS Behavioral Modelling and Simulation of High- Pass Delta-Sigma Modulator

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Context

“Digital designers to take over the world when analog designers produce 10 Gbps 18-bit data converters that attach to antennas”

✧ Wide band conversion : Software radio and cognitive radio

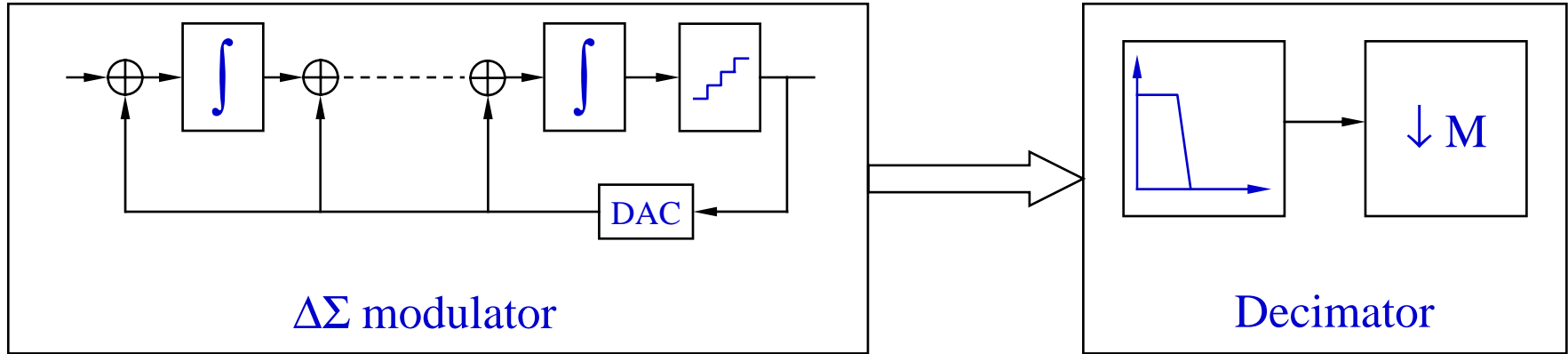
- Parallel architecture : high speed
- Delta-sigma converter : high resolution
- Parallel delta-sigma converter :
 - Time-interleaved delta-sigma converter
 - High-pass delta-sigma modulator

- ✧ **High-Pass Delta-Sigma Modulator**
 - **Operation Principle**
 - **SC High-Pass Filter**
 - **Key Parameters**

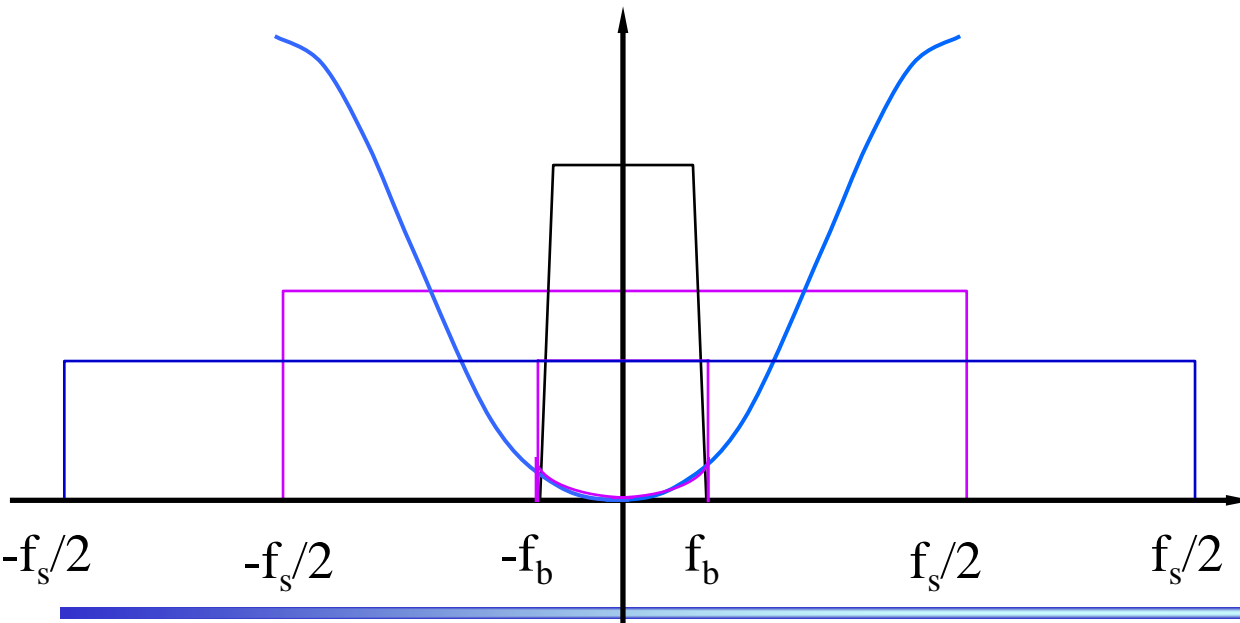
- ✧ **VHDL-AMS Modelling and Simulation**
- ✧ **Simulation vs measurement results**

- ✧ **Conclusion**

Delta-Sigma Modulator



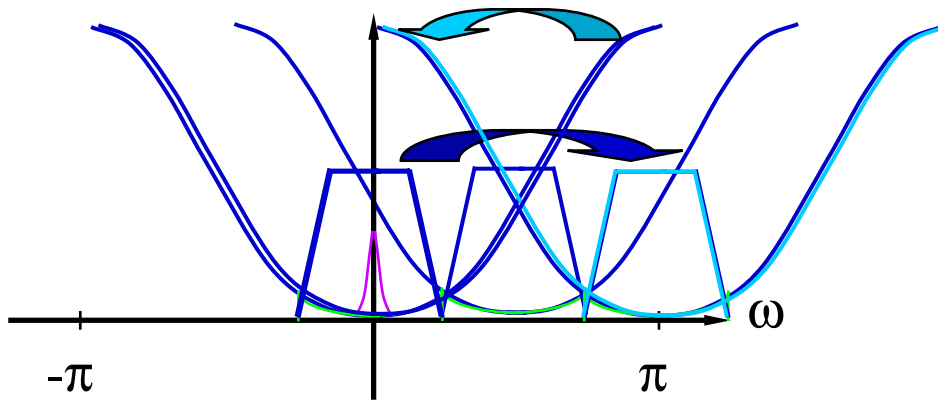
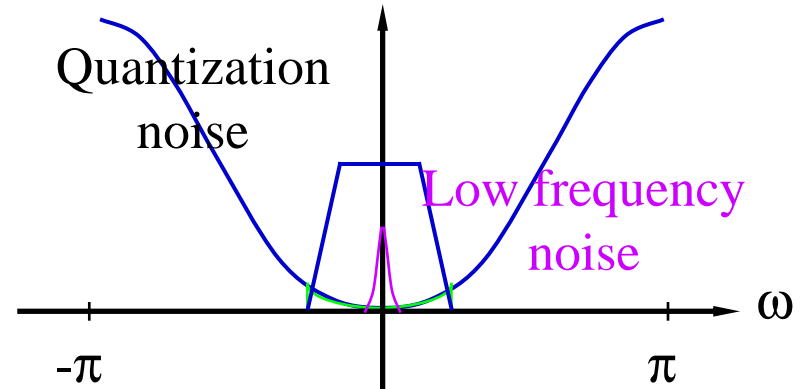
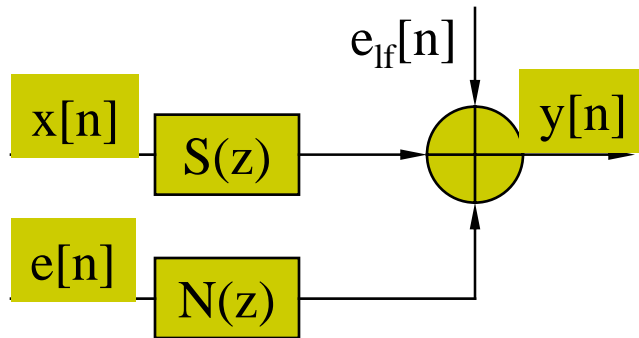
- Principles : Oversampling + Noise shaping



- Parameters :
 - Modulator order : number of integrators
 - OSR
 - Number of bits of quantizer
- Performance : $6L+3$ dB/Octave

Delta-Sigma Modulator

- **Low frequency noise effect**



Integrator

$$\frac{z^{-1}}{1-z^{-1}}$$

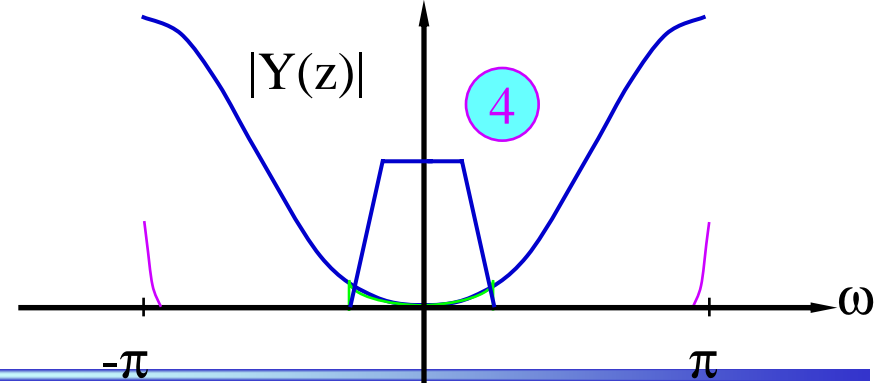
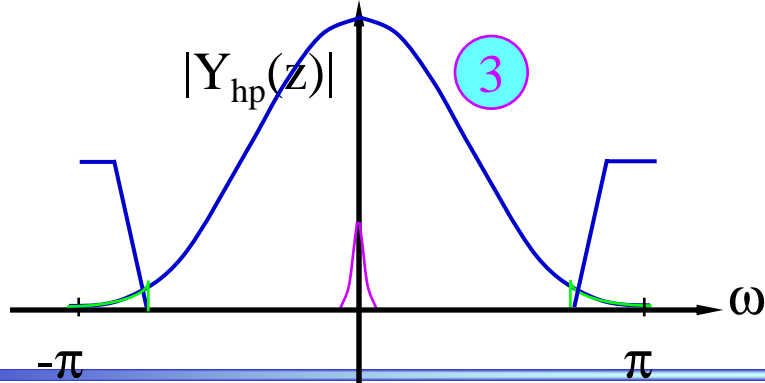
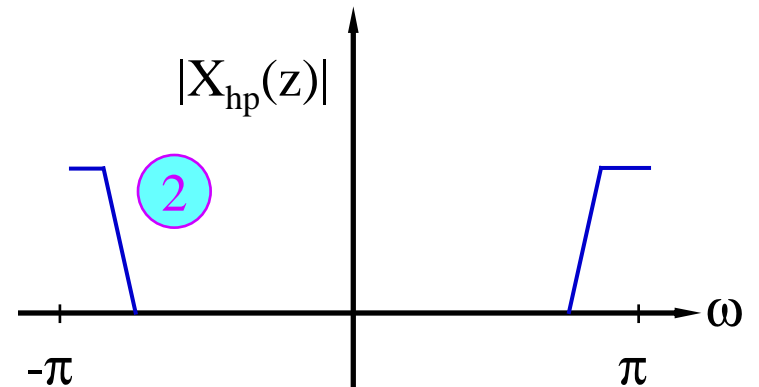
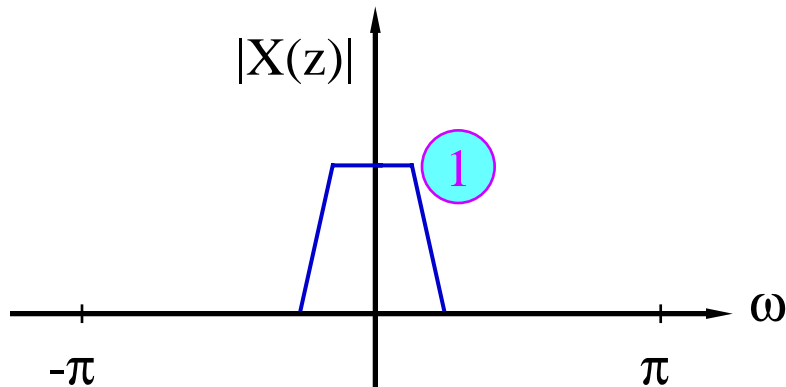
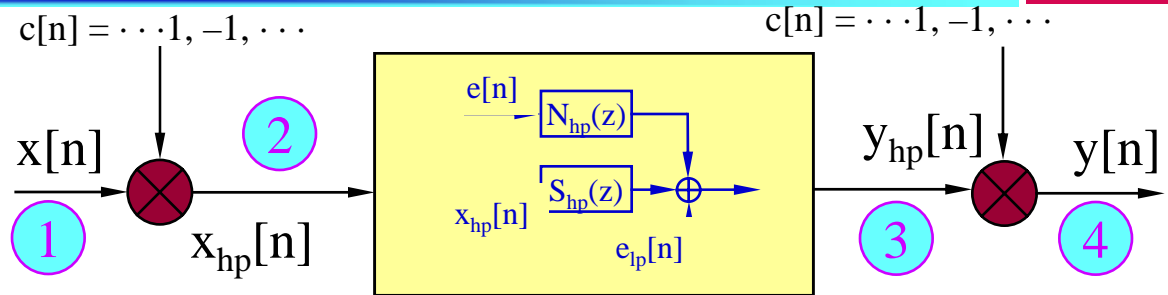
$$z \rightarrow -z$$

High-pass filter

$$\frac{z^{-1}}{1+z^{-1}}$$

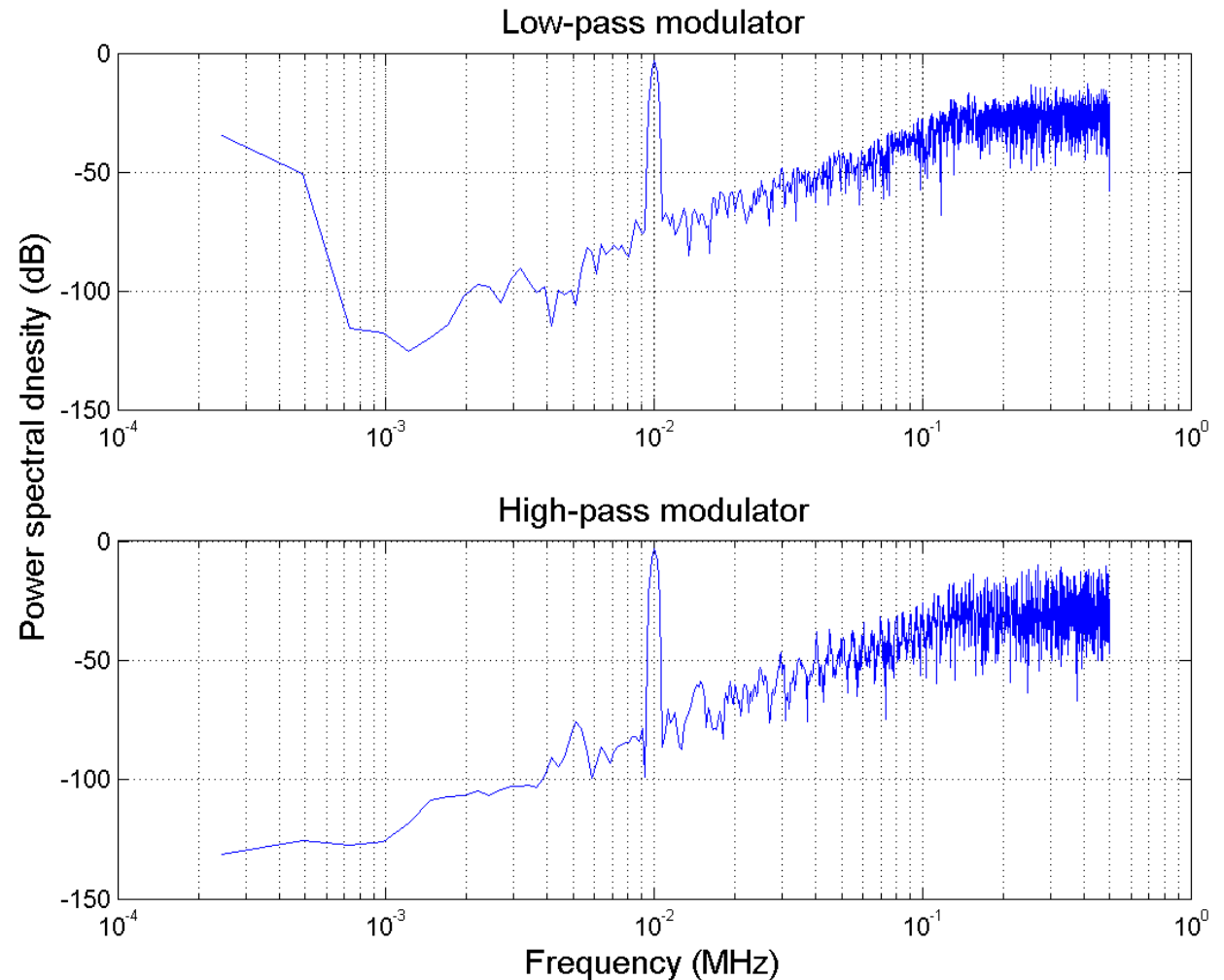
High-Pass Delta-Sigma Modulator

- Low frequency noise effect



High-Pass Delta-Sigma Modulator

- **Assumption:**
quantization noise is additive white noise and uncorrelated with input signal
- **Spectrum of modulators output**
 - In the presence of low frequency noise
 - Input frequency : 10 KHz
 - Sampling frequency : 1 MHz

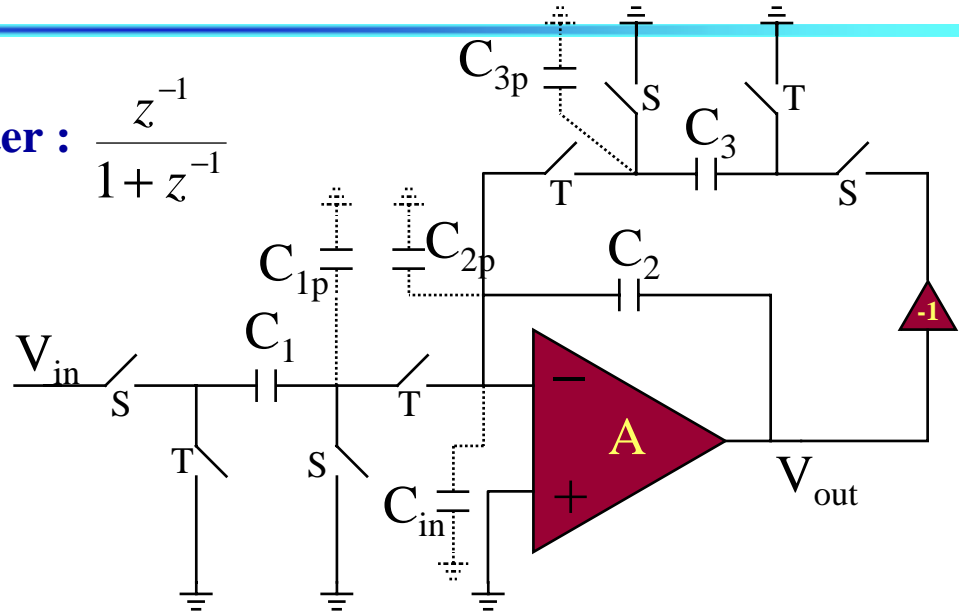


High-Pass Delta-Sigma Modulator

- SC implementation of high-pass filter : $\frac{z^{-1}}{1+z^{-1}}$

$$H(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1-z^{-1}}$$

$$H_{hp}(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1 + \frac{C_3 - C_2}{C_2} z^{-1}}$$



$$C_3 = 2 \times C_2$$

$$H_{hp}(z) = \frac{C_1}{C_2} \frac{(1-\alpha)z^{-1}}{1+\beta z^{-1}}$$

$$\alpha \approx \frac{1}{A} \left(1 + \frac{C_1 + C_2 + C_3 + C_{para}}{C_2} \right)$$

$$\beta \approx \frac{\frac{C_3 - C_2}{C_2} \frac{C_2 + C_{para}}{AC_2}}{1 + \frac{C_1 + C_2 + C_3 + C_{para}}{AC_2}} \leq \frac{C_3}{C_2} - 1$$

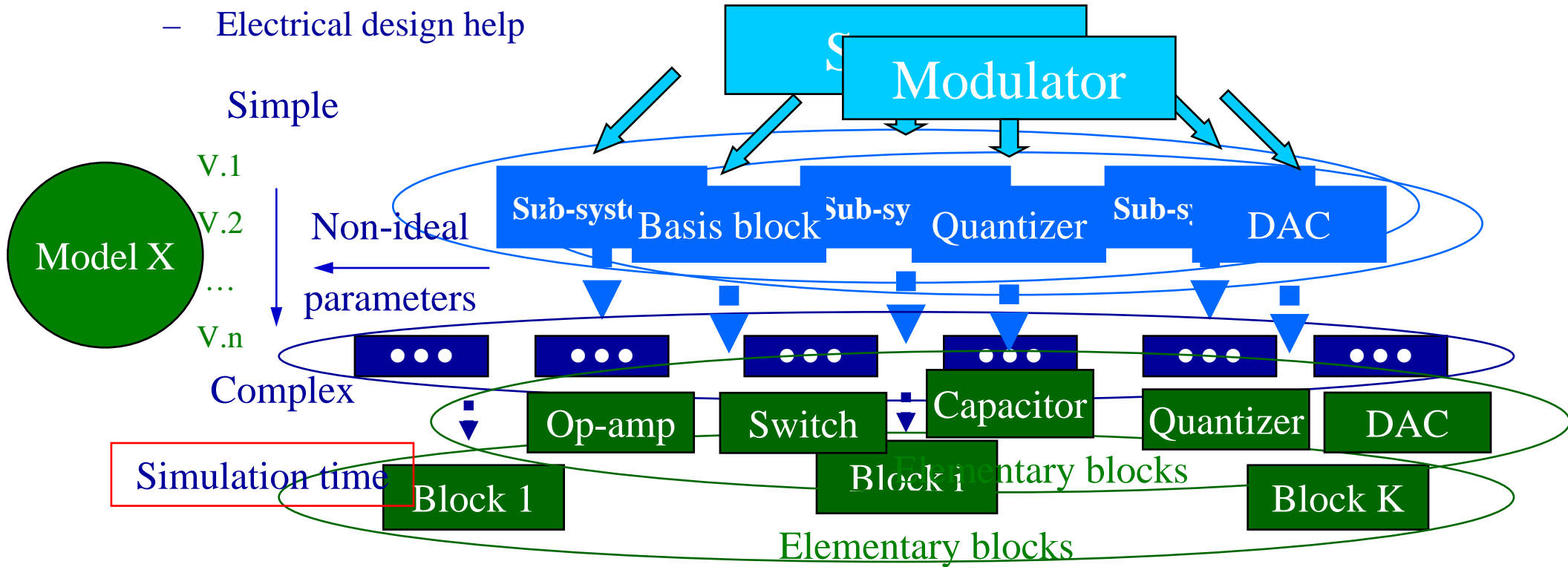
Stability :

Error on $C_3/C_2 < 2.4\%$

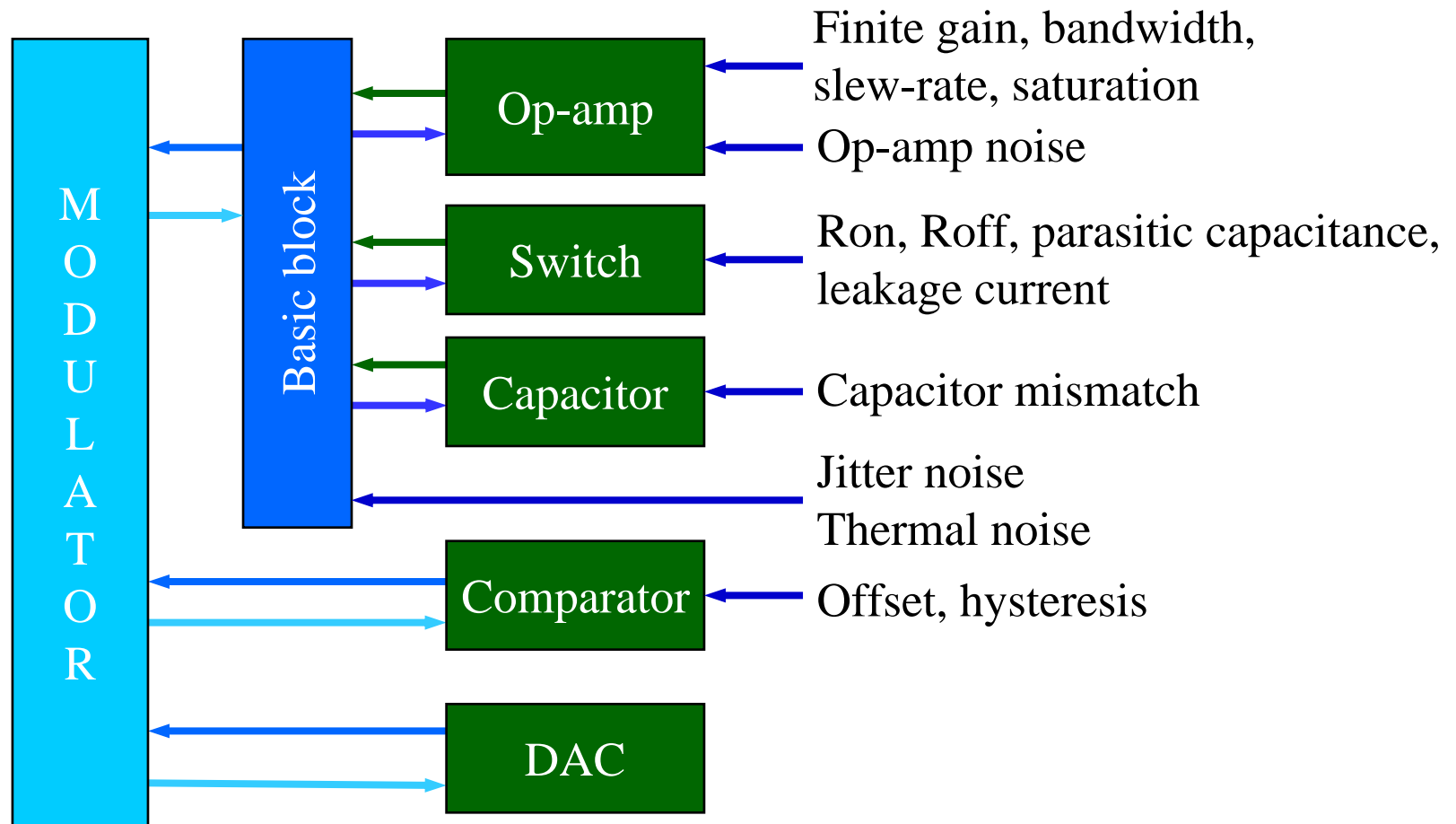
Performance :

Error on $C3/C2 < 1\%$

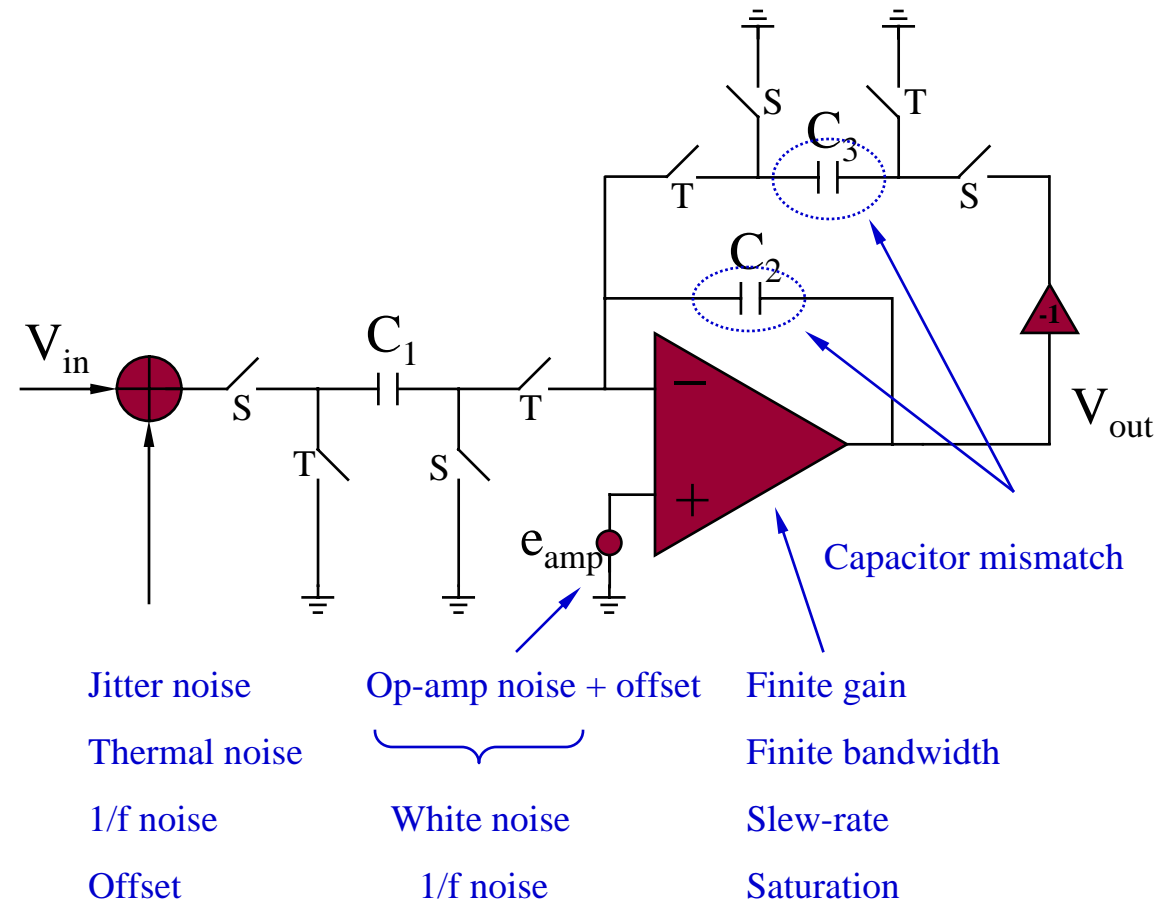
- Objectives :
 - Effect of different non-ideality parameters on modulator performance
 - Threshold of non-ideal parameters to ensure a good performance of the modulator
 - Reduction of simulation time
 - Electrical design help



- Modelling and simulation



- Complete high-pass filter model
- Modulator model
 - Complete model of the first high-pass filter
 - Second high-pass filter model without noise
- Non-ideality and noise effect
 - Noises : increased inband noise level
 - Op-amp non-ideality : distortion, stability
 - Capacitor mismatch : stability
 - Switch resistance : inband noise

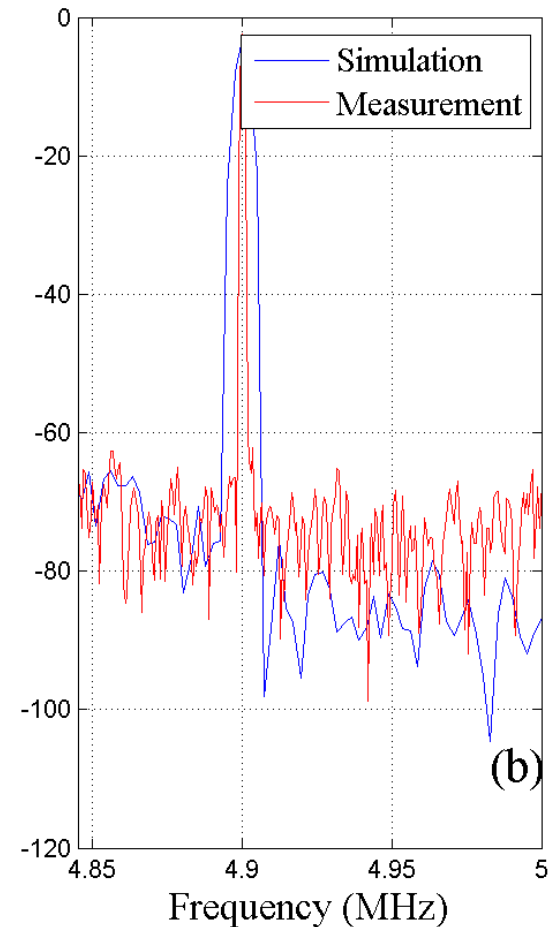
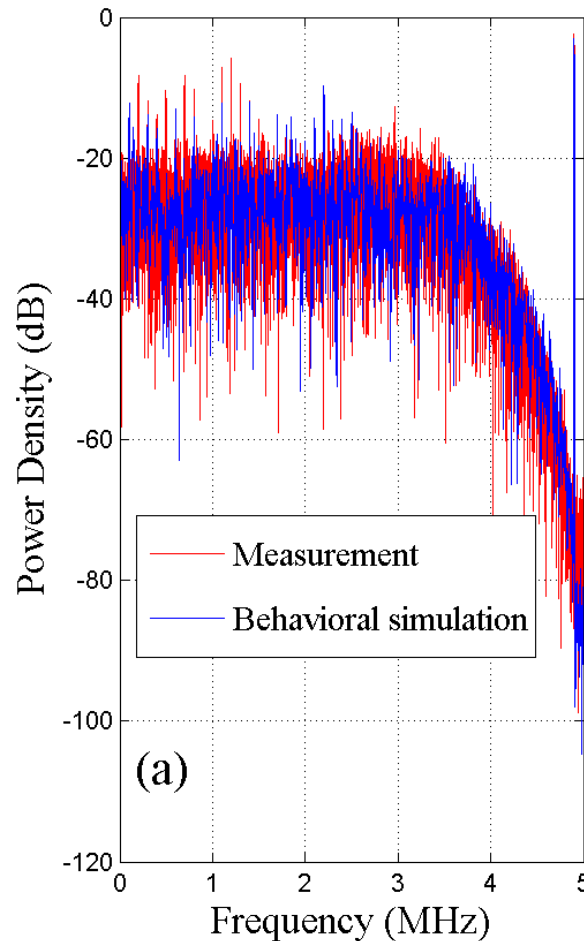


- **Specification summary**

Nonideality	Parameter	Threshold value
Sampling jitter	ΔT	< 0.1 ns
Switch noise (KT/C)	C	> 10 fF
Amplifier noise	E_{amp}	< 0.2 mVrms
Switch on-resistance	R_{on}	< 1 K Ω
Parasitic switch capacitance	$C_{rec+WLCox}$	< 30 fF
Leakage current	I_{fd}	< 0.1 μA
Finite gain	Gain	> 60 dB
Transition frequency	F_t	> 160 MHz
Slew-rate	SR	> 50 V/ μs
Saturation	V_{max}	> 1.4 V
Capacitor mismatch	C_3/C_2	< 0.5 %

Simulation vs Measurement Results

- Second order high-pass delta-sigma modulator
- Input @ 10KHz
- F_s : 10MHz
- OSR : 32
- SNR : 53dB
- SNDR : 51 dB



✧ **Design methodology with VHDL-AMS**

- Set of model to simulate $\Delta\Sigma$ modulator
- Effect of non-ideal parameter
- Noises effect on the modulator performance
- Block specification
- Optimization for low-pass $\Delta\Sigma$ modulators