

Hierarchical Symbolic Piecewise-Linear Circuit Analysis

Junjie Yang, Sheldon X.-D. Tan, Martin Gawecki

Mixed-Signal Nanometer VLSI Lab.
Department of Electrical Engineering
University of California at Riverside





Outline

- Introduction
- Background of the proposed algorithm
 - Parameterized Representation of PWL Devices
 - Time-Domain DDD Graphs
 - The Hierarchical Symbolic Analysis for PWL Circuits
 - Review of general Katzenelson's algorithm
- New Hierarchical Transient Analysis of PWL Circuits
- Experiments and Results
- Conclusion



Introduction—Piece Wise Linear

- **PWL Modeling**

- Use piecewise-linear approximation for modeling nonlinearity
- Describe general (weakly or hard) nonlinear behavior

- **Why choosing PWL?**

- Model the different-level components in a uniform way
- PWL algorithms have excellent convergence properties, especially for hard nonlinear circuits

Introduction--PWL

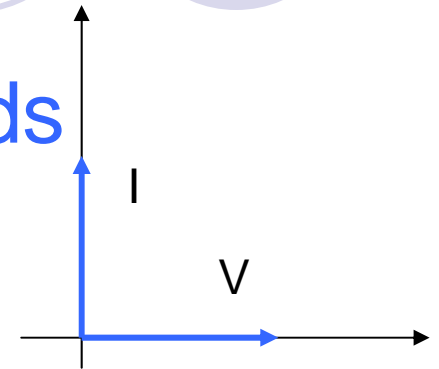
- Two kinds PWL simulation methods

- Pure numerical methods

- Ideal-diode based methods
- Large circuit causes big matrix and will increase simulation time (with or without ideal-diode)

- Symbolic analysis methods

- Mathematica-based method (Filippetti'00)
- Behavioral Modeling (Fernandez'98)
- Complimentary Decision Diagram (Manthe'03)



Introduction—the proposed new approach

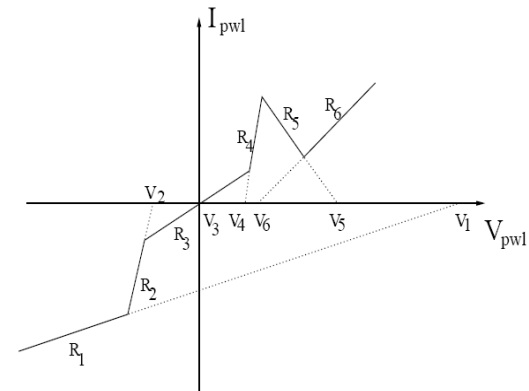
- General hierarchical piecewise symbolic analysis approach
 - Parameterized PWL modeling $f(x) = a_i x + b_i$
 - Compact compared with ideal-diode based circuit
 - Hierarchical symbolic analysis
 - Allow much larger nonlinear analog circuits
 - Event-driven (Katzenelson's method) PWL analysis scheme

Parameterized Representation of PWL Devices

- For PWL I-V curve of a two-terminal device, the MNA stamp can be written as

$$\begin{array}{c} n_1 \\ n_2 \\ n_{pwl} \end{array} \left[\begin{array}{cc|c} n_1 & n_2 & n_{pwl} \\ \hline & & 1 \\ & & -1 \\ 1 & -1 & -R_i \end{array} \right] \begin{bmatrix} V_{n_1} \\ V_{n_2} \\ I_{pwl} \end{bmatrix} \begin{bmatrix} \\ \\ V_i \end{bmatrix}$$

- R_i is the reciprocal of the slope of the i th segment
- V_i is its intercept with x-axis
- PWL component can reduce MNA size compared to ideal diode model



Parameterized Representation of PWL Devices

- The stamps of PWL voltage-controlled voltage source

$$\begin{array}{c}
 n_1 \\
 n_2 \\
 n_3 \\
 n_4 \\
 n_{pwl}
 \end{array}
 \left[\begin{array}{cccc|c}
 n_1 & n_2 & n_3 & n_4 & n_{pwl} \\
 & & & & 1 \\
 & & & & -1 \\
 & & & & 0 \\
 & & & & 0 \\
 \hline
 -R_i & R_i & 1 & -1 & 0
 \end{array} \right]
 \begin{bmatrix}
 V_{n_1} \\
 V_{n_2} \\
 V_{n_3} \\
 V_{n_4} \\
 I_{pwl}
 \end{bmatrix}
 \begin{bmatrix}
 \\
 \\
 \\
 \\
 V_i
 \end{bmatrix}$$

- PWL voltage-controlled current source

$$\begin{array}{c}
 n_1 \\
 n_2 \\
 n_3 \\
 n_4 \\
 n_{pwl}
 \end{array}
 \left[\begin{array}{cccc|c}
 n_1 & n_2 & n_3 & n_4 & n_{pwl} \\
 & & & & 1 \\
 & & & & -1 \\
 & & & & 0 \\
 & & & & 0 \\
 \hline
 0 & 0 & 1 & -1 & -R_i
 \end{array} \right]
 \begin{bmatrix}
 V_{n_1} \\
 V_{n_2} \\
 V_{n_3} \\
 V_{n_4} \\
 I_{pwl}
 \end{bmatrix}
 \begin{bmatrix}
 \\
 \\
 \\
 \\
 V_i
 \end{bmatrix}$$

Parameterized Representation of PWL Devices

- General equations for a PWL circuit is

$$Hx = b$$

- H is the PWL circuit matrix
- X is the circuit unknown vector
- b is system excitations like current sources
- Advantage: all the linear symbolic / numerical techniques can be used to solve PWL matrix easily

Time-Domain DDD Graphs

- DDD (determinant decision diagrams)
 - The leading symbolic analysis method
 - The hierarchical approach using DDD graphs can be used in arbitrary large linear circuits
- In this paper, we built a time-domain DDD to do symbolic transient analysis
 - According to PWL components, get different stamps for all the unknown in the circuits
 - Get unknown vector x_k by

$$H_k = \begin{bmatrix} a_{1,1} & \dots & a_{1,k-1} & b_1 & a_{1,k+1} & \dots & a_{1,n} \\ a_{2,1} & \dots & a_{2,k-1} & b_2 & a_{2,k+1} & \dots & a_{2,n} \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ a_{n,1} & \dots & a_{n,k-1} & b_n & a_{n,k+1} & \dots & a_{n,n} \end{bmatrix} \quad x_k = \frac{\det(H_k)}{\det(H)}$$

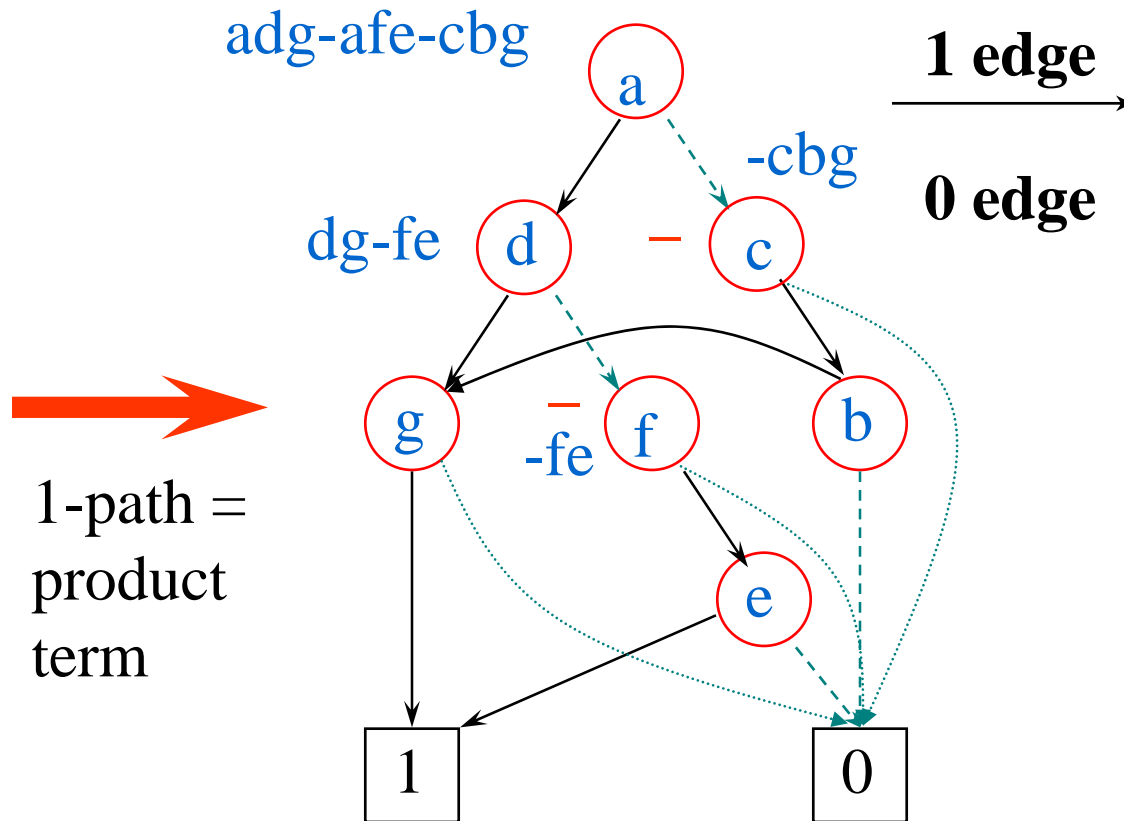
Time-Domain DDD Graphs--Example

$$a(s) = \frac{1}{R_1} + sC_1 + \frac{1}{R_2}$$

a	b	0
c	d	e
0	f	g

Product terms:

$adg, -afe, -cbg$



The Hierarchical Symbolic Analysis for PWL Circuits

- Schur decomposition method

$$\begin{bmatrix} A^{II} & A^{IB} \\ A^{BI} & A^{BB} \\ & A^{RB} & A^{RR} \end{bmatrix} \begin{bmatrix} x^I \\ x^B \\ x^R \end{bmatrix} = \begin{bmatrix} b^I \\ b^B \\ b^R \end{bmatrix} \quad \longrightarrow \quad \begin{bmatrix} A^{BB^*} & A^{BR} \\ A^{RB} & A^{RR} \end{bmatrix} \begin{bmatrix} x^B \\ x^R \end{bmatrix} = \begin{bmatrix} b^{B^*} \\ b^R \end{bmatrix}$$
$$A^{BB^*} = A^{BB} - A^{BI} (A^{II})^{-1} A^{IB}$$
$$b^{B^*} = b^B - A^{BI} (A^{II})^{-1} b^I$$

- We apply this hierarchical symbolic analysis to obtain exact symbolic solution of PWL circuit matrices

Review of general Katzenelsohn's algorithm

- Katzenelsohn's algorithm is widely used in PWL DC and transient analysis $H^m x + w^m = y$
- Consider a flat PWL circuit for which the equation can be written as $H^m x_0 + w^m = y_0$
 - H^m is the system matrix for *m*th linear region
 - Suppose there is an initial solution x_0 made

Review of general Katzenelsohn's algorithm

- Δy_k represents the error vector of right-hand side at kth step

$$\Delta y_k = H_k^m x_k + w_k^m - y = H_k^m \Delta_k$$

- If the final solution in this linear region

$$x = x_k + \Delta x$$

- If any component crosses into a new linear region

$$x_{k+1} = x_k + \lambda \Delta x_k \quad 0 < \lambda < 1$$

- λ is to make sure there is only one component crossing into a new region at one time

New Hierarchical Transient Analysis of PWL Circuits

- Combine Katzenelson's algorithm with hierarchical symbolic method
- Perform transient analysis
- The object is hierarchical piecewise linear circuits

New Hierarchical Transient Analysis of PWL Circuits

- The details of the new algorithms:
 - Build symbolic expressions
 - The object: all the subcircuit and top level circuit in a bottom up way
 - In the terms of DDD graphs according to the equations below

$$H^{BB^*} = H^{BB} - H^{BI} (H^{II})^{-1} H^{IB}$$

and

$$H^{II} x^I = b^I - H^{IB} x^B$$

New Hierarchical Transient Analysis of PWL Circuits

- At the top level circuit, formulate the equations below

$$H_k^m \Delta x_k = \Delta y_k$$

- Δy are symbolic expressions
- Δy is composed of independent sources and the source of reactive elements' companion models

New Hierarchical Transient Analysis of PWL Circuits

- When $t=t_n$
 - All input sources and the current and voltage sources associated with reactive components are updated
 - Use linear region variables to update matrix H_k^m
 - t_{n-1} as the initial solution
 - At $t=0$, $x_0=0$ and $y_0=0$
 - $\Delta y=y-y_0$ and compute the right hand sides for all middle circuits and root circuit.
 - Solve the root circuit

New Hierarchical Transient Analysis of PWL Circuits

- When $t=t_n$

- Obtain Δx with $H_k^m \Delta x_k = \Delta y_k$, and get all solutions of leaf circuits in a top-down way
- Compute λ , which meet $0 < \lambda \leq 1$
$$\lambda = \min(\lambda_i) \quad \lambda_i = \frac{(x_i^b - x_i)}{\Delta x_i}$$
- Update the solution for the roof circuit and all subcircuits with the equations below

$$x_0 = x_0 + \lambda \Delta x$$

$$y_0 = y_0 + \lambda \Delta y$$

New Hierarchical Transient Analysis of PWL Circuits

- When $t=t_n$
 - When $\lambda = 1$, x_0 is the final solution at the time $t=t_n$
 - Otherwise, switch to the new linear region of the PLW component, compute with updated matrix H_k^m until $\lambda = 1$.
- Go to next time point $t=t_{n+1}$

New Hierarchical Transient Analysis of PWL Circuits

- The features of the new algorithm
 - We only need to build the symbolic expression only once and evaluate them for many times
 - The improved Katzenelson's algorithm is guaranteed to converge as all the linear region will be searched after sufficient events



Experiments and Results

- Experiment environment:

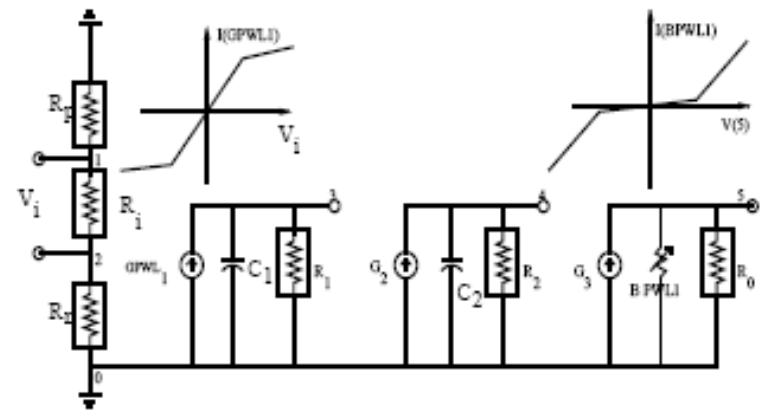
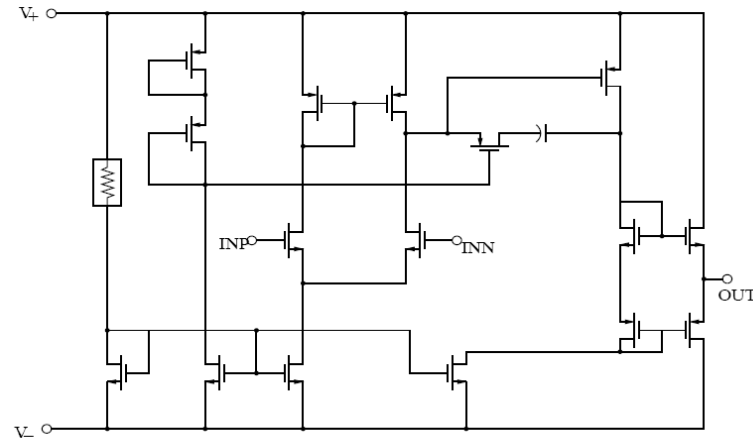
- Linux PC with 2.4Ghz CPU and 484M RAM

- Experiment circuit

- A Pulse-Width-Modulated (PWM) system
- Band-pass circuit
- Low-pass circuit

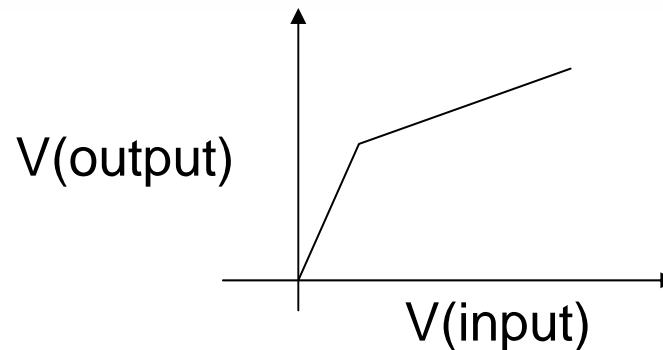
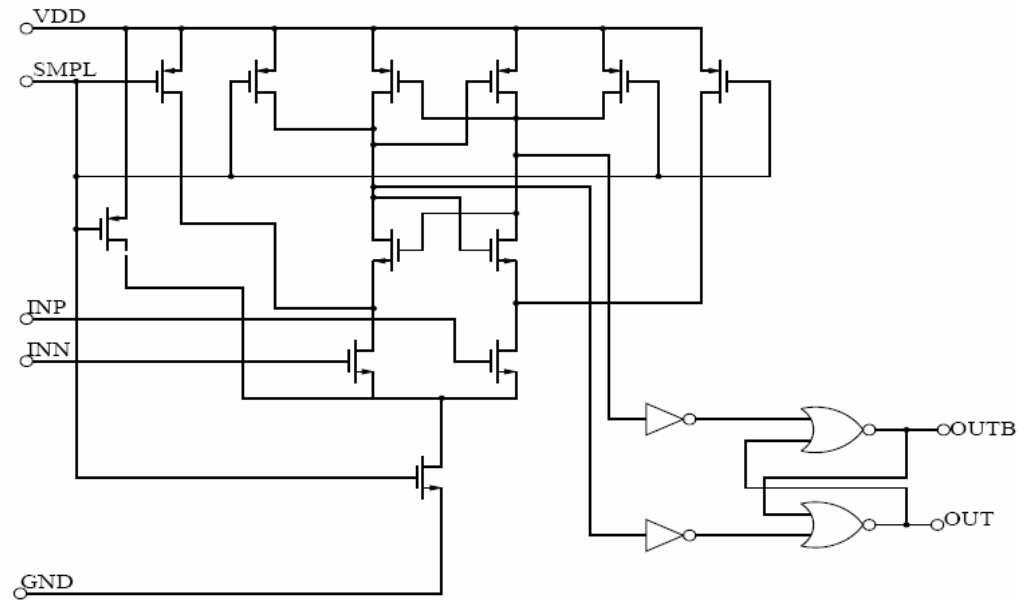
Experiment—PWM System

- The implementation of OPAMP
 - Include GPWL1 for slew rate limiting and BPWL1 for output clamping
- Extract its behavioral model
 - Conduct DC sweeping and AC analysis
 - Obtain gain, finite output swing etc



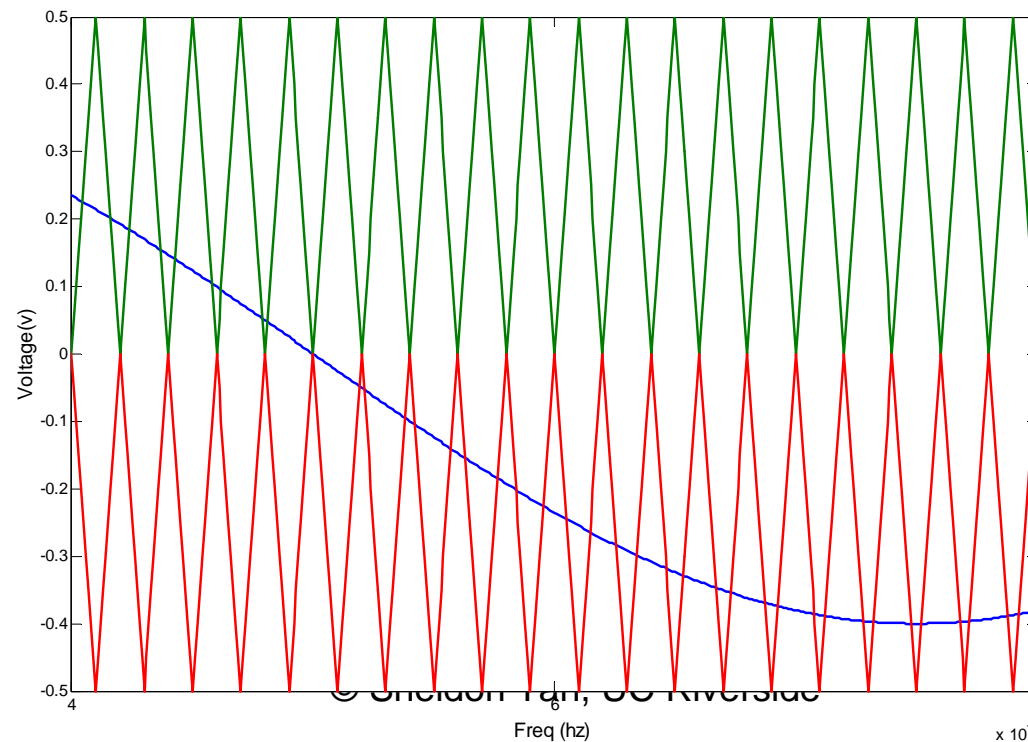
Experiment—PWM System

- Comparator implementation circuit
- It is replaced by a piecewise-linear voltage-controlled voltage source as its behavioral model



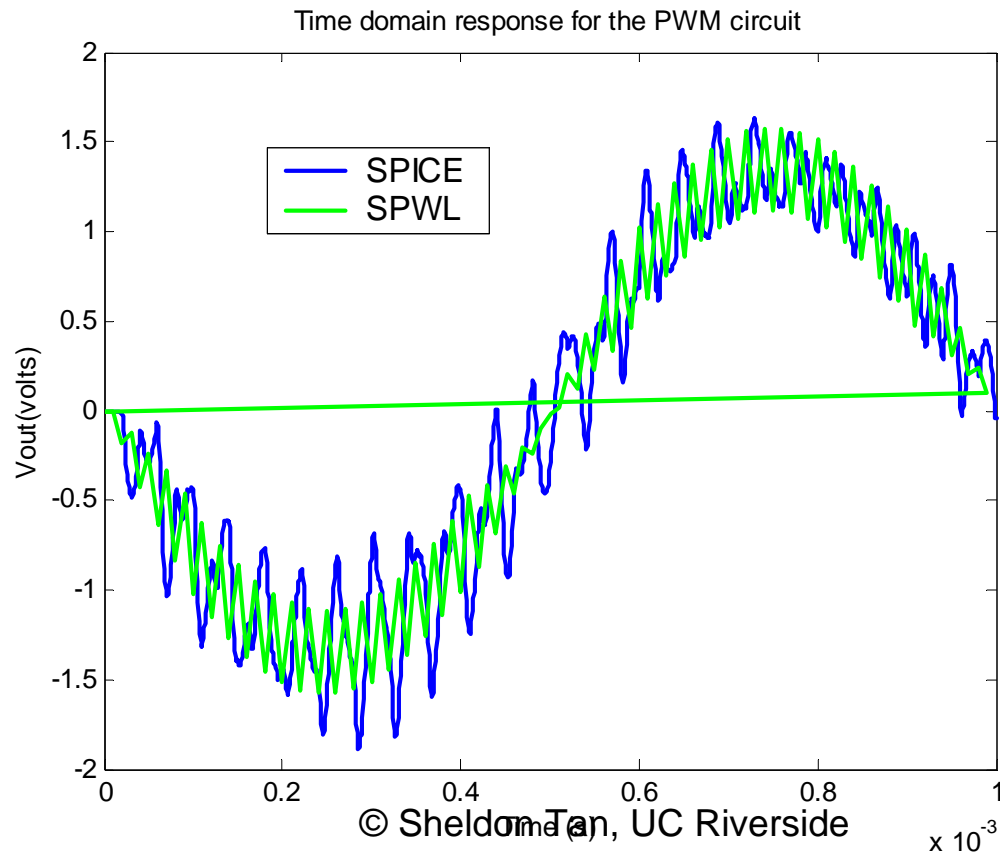
Experiment—PWM System

- Input: upper and down triangle waves
- Advantage: save power
 - When output signal is zero when input is zero



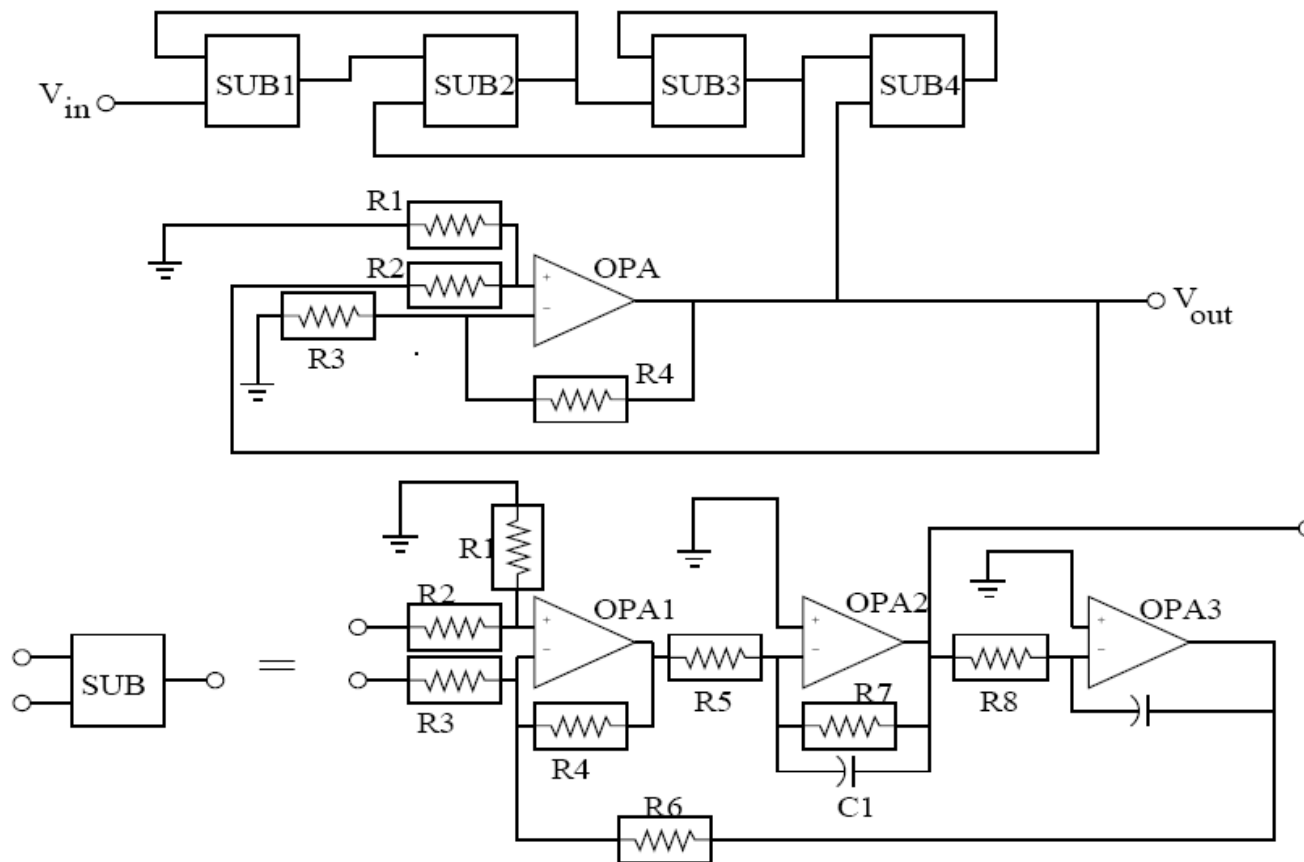
Experiment—PWM System

- Compare our PWL tools and SIMetrix simulator
 - PWL tools include SPWL-flat and SPWL-hier tools



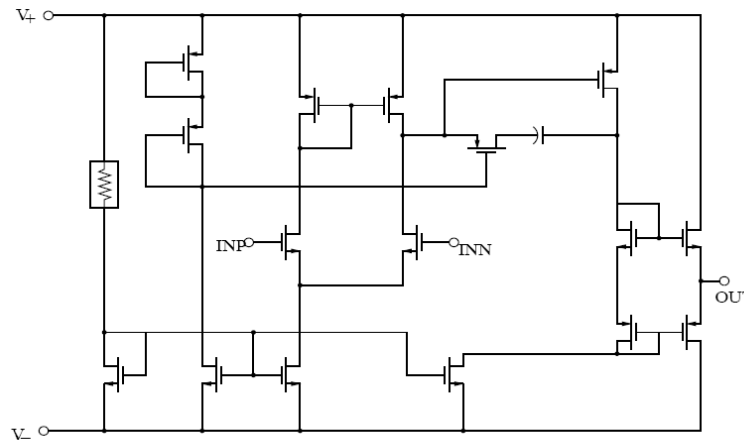
Experiment—Band-pass circuit

- The schematic of this circuit



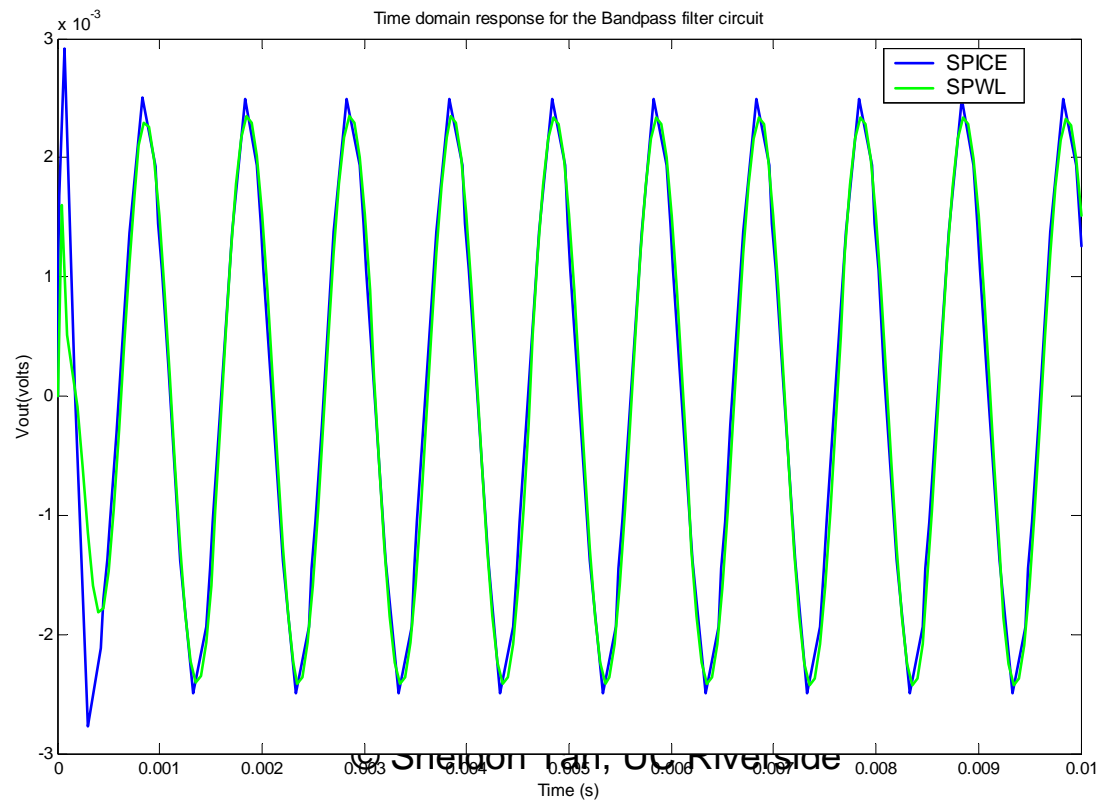
Experiment—Band-pass circuit

- Use the same figure as the previous example as its behavioral model of PWL simulation
- The actual circuit implementation of OPAMP



Experiment—Band-pass circuit

- The transient responses from SIMatrix and PWL tools are shown below



Experiment--timing cost

- The CPU time of both PWM, Low-pass and Band-pass are shown in the table
- They delivers about 10X speedup over SIMetrix
- Hierarchical PWL simulation is 3X to 5X faster than the flat one and can manage larger circuits

Circuits	SIMetrix	SPWL-flat	SPWL-hier
PWM	342s	290.74s	67.61
LowPass	306s	125.02s	44.04s
BandPass	317s	N/A	36.75s



Conclusion

- Propose a new approach for hierarchical transient analyses for nonlinear circuits modeled as PWL circuit
- Propose parameterized PWL modeling
 - Solved the circuits symbolically using hierarchical DDD only once
 - Evaluated many times in Katzenelson method
- New algorithm outperforms SIMetrix in CPU times with reasonable accuracy