

Improved Phase Noise Model for Ultra Wideband VCO

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ABSTRACT

An improved phase noise model for an ultra wideband differential voltage controlled oscillator is proposed which accurately models the impact of tuning voltage on phase noise performance. A series of design examples are presented, which indicate that results from the proposed model agree strongly with transistor level simulations. The model has been further extended to single ended structures where further design examples indicate that accuracy is maintained.

1. INTRODUCTION

Voltage controlled oscillators (VCOs) are an essential building block in many integrated circuits and are typically based on either a passive inductor-capacitor (LC), or a delay cell ring structure. The advantages of wide tuning range, small chip area and compatibility with standard digital processes make the delay cell based ring structures popular for applications where phase noise is less critical. It is important to be able to model the phase noise and jitter of inverter based VCOs in order to facilitate accurate performance estimation during the design stage. A number of models were proposed in the 1990s which provided some basis for phase noise prediction but were not sufficient to allow a designer to make transistor sizing decisions [1]-[4].

Some commercially available simulation tools have accurate phase noise and jitter analysis functionality built in. However, simulation times can be excessive, often running into several hours for a single measurement. Recent work has attempted to solve this problem by developing a direct relationship between the phase noise performance and the VCO delay cell transistor sizing [5][6]. However, these do not take into account the impact of the tuning mechanism on the noise performance and so are only valid at the highest frequency of operation.

The delay cell and VCO structure used for this model are shown in Figure 1(a) and (b). Frequency tuning of the delay cell is achieved through the two differential control signals V_p and V_n . Adjusting these voltages changes the amplitude of currents I_1+I_2 and I_3 which in turn alters the output frequency. This adjustment in I_1+I_2 and I_3 impacts on the phase noise figure, but most previous models ignore this factor and assume a fixed frequency of operation [2][5]. One might consider that since phase noise increases with increasing frequency, but decreases with smaller current consumption, the noise level increment due to the decreasing current is compensated by the simultaneous reduction in oscillation frequency. However, over a wide tuning range, this assumption does not hold true due to the non-linearity of the active devices used. This paper presents an improved phase noise model for the ultra wideband inverter based VCO shown in Figure 1 [7]. The new model directly relates transistor dimensions to phase noise performance and unlike previous work, takes into account the impact of the tuning voltage on the noise performance.

The paper is organized as follow. The proposed improved phase noise model is developed in Section 2. A series of examples, which compare theory and simulation, are given in Section 3. Finally, Section 4 extends the model to single ended structures giving further results to confirm the accuracy of the model. Concluding remarks are given in Section 5.

2. IMPROVED PHASE NOISE MODEL

Considering the delay cell shown in Figure 1, equation (1) is used to relate the dimensions of Mn1 to the dimensions of Mp1 and Mp3 [7]. The parameters V_{tn} and V_{tp} are the transistor threshold voltages and μ_p and μ_n are their mobility parameters. The cascode devices Mp2 and Mn2 are given the same dimensions as Mp1 and Mn1 respectively and the opposite side of the delay cell is sized in an identical manner.

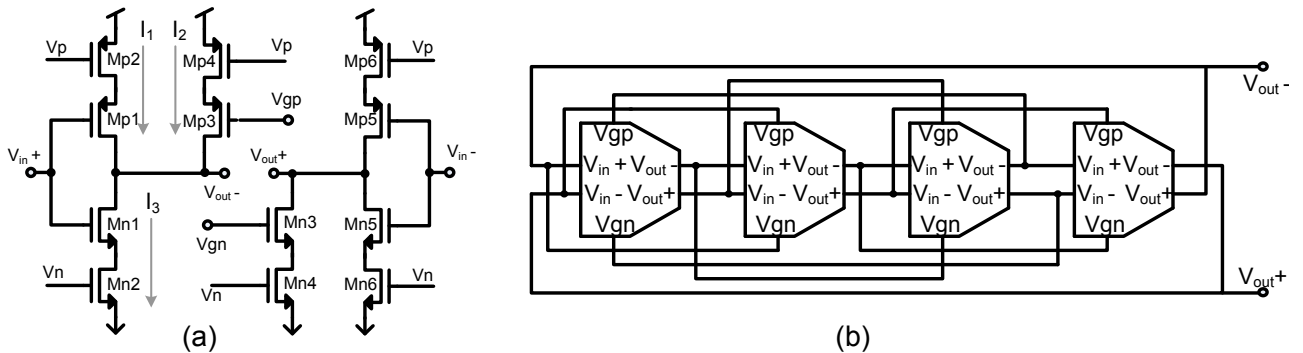


Figure 1 Improved double feedback dual inverter delay cell (a) and VCO architecture (b)

$$\left(\frac{W}{L}\right)_{n1} = \frac{\mu_p}{\mu_n} \left[\frac{\frac{V_{DD}}{2} - |V_{tp}|}{\frac{V_{DD}}{2} - |V_{tn}|} \right]^2 \left[\left(\frac{W}{L}\right)_{p1} + \left(\frac{W}{L}\right)_{p3} \right] \quad (1)$$

Furthermore, the branches on the left (Mn1) and right (Mp5) side of the delay cell should carry equal current, giving:

$$W_{p1} + W_{p3} \approx W_{p5} \quad W_{n5} + W_{n3} \approx W_{n1} \quad (2)$$

Two simplifications can be made for the remaining analysis, both of which have little impact on the model accuracy. Firstly, the differential structure is considered as a single ended structure with twice as many stages and secondly the left side of the delay cell, shown in Figure 2.a, can be simplified to that of Figure 2.b. As a result, an N stages dual inverter delay cell based VCO can be modeled as a loop of 2N of the single ended delay cells shown in Figure 2.b.

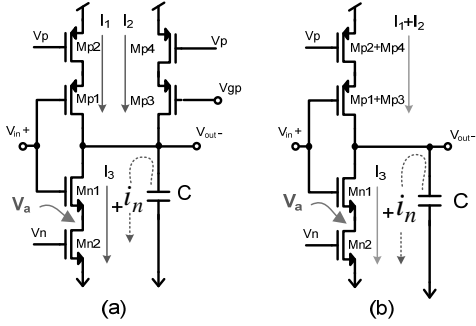


Figure 2 Theoretical model for proposed delay cell

The propagation time, t_d , of the delay cell is defined as the time taken for a change in the input to propagate to the output, and this is normally measured as the time between $V_{dd}/2$ crossing points. Figure 3 shows the simulated input and output waveform for an example transition. Assuming the drain current (I_3) of Mn1 is constant during the increase of the input voltage, the time delay, t_d , can be found from equation(3), where C is the gate capacitance of the next stage of loop.

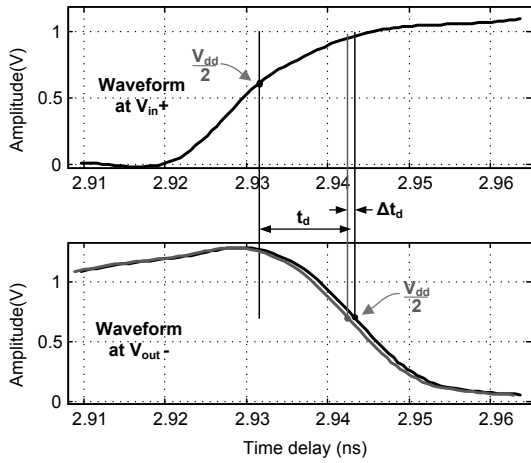


Figure 3 Propagation delay variation for proposed delay cell

$$t_d = RC = \frac{V_{dd}C}{2I_3} \quad (3)$$

However, in addition to the pull down current I_3 , a noise current i_n may be integrated on the load capacitor C over the time window t_d . This generates a noise induced voltage, v_n , which leads to a fluctuation in the propagation delay, defined as Δt_d . This delay fluctuation can be seen in Figure 3 as a time domain shift in the output waveform. Only the flicker noise of the devices are considered, since this dominates the phase noise spectrum up to few MHz. The spectral density of the flicker noise induced Δt_d is given in previous work [6] as:

$$S_{\Delta t_d}(f) = \frac{t_d^2}{I_3^2} \text{sinc}^2(\pi f t_d) \times \frac{K_f}{WLC_{ox}} \frac{1}{f} g_m^2 \quad (4)$$

However, as already discussed, this equation does not take into consideration the effect of tuning voltage on phase noise performance due to the change in I_3 , and this is now considered as part of the improved model. From theory and extensive simulations it has been confirmed that since the cascode transistors (Mn2, Mp2, and Mp4) work in the deep triode region they contribute little to the overall noise. The main noise contribution therefore comes from the current starved transistors (Mn1, Mp1, and Mp3) as they are working in the saturation region. Using the square law for transconductance, $g_m = 2I/V_{eff}$, equation (4) can be written again as:

$$S_{\Delta t_d}(f) = \left(\frac{I_{n1}^2}{I_3^2}\right) \text{sinc}^2(\pi f t_d) \times \frac{K_f}{W_{n1}L_{n1}C_{ox}} \frac{1}{f} \frac{4t_d^2}{(V_{dd} - V_m)^2} \quad (5)$$

Here, I_{n1} is modeled as the Mn1 drain current when the cascode transistor Mn2 is at its minimum resistance. Provided that Mn1 and Mn2 have the same dimensions and if $V_n = V_{dd}$, then I_{n1} should equal the maximum achievable value of I_3 . Therefore, a new coefficient, P , is introduced as the ratio of I_{3max} to its instantaneous value I_{3inst} , as controlled by V_n . Using standard first order equations for a transistor in the triode region, the coefficient P can be related to the oscillator tuning voltage V_{ninst} as follows:

$$P = \frac{I_{3max}}{I_{3inst}} = \frac{V_{nmax} - V_m - V_a / 2}{V_{ninst} - V_m - V_a / 2} \quad (6)$$

where V_a is the drain voltage of transistor Mn2 as shown in b. Simulation results show that V_a varies linearly with the channel length L_{n1} . Based on extensive simulations, the relation $V_a \approx ((L_{n1} - L_{min})/L_{min})V_m$ makes a good approximation for the proposed model over the majority of the tuning range. Thus, equation (6) can be written as equation (7) where L_{min} is the minimum allowable transistor length. Equation (5) can also be written again as equation (8).

$$P = \frac{I_{3max}}{I_{3inst}} = \frac{V_{nmax} - ((L_{min} + L_{n1})/2L_{min})V_m}{V_{ninst} - ((L_{min} + L_{n1})/2L_{min})V_m} \quad (7)$$

$$S_{\Delta t_d}(f) = P^2 \left(\frac{I_{n1}^2}{I_{3max}^2}\right) \text{sinc}^2(\pi f t_d) \frac{K_f}{W_{n1}L_{n1}C_{ox}} \frac{1}{f} \frac{4t_d^2}{(V_{dd} - V_m)^2} \quad (8)$$

The coefficient P shows the impact of the tuning voltage on the noise. Finally, the SSB phase noise, $\mathcal{L}(f)$, and hence the improved phase model can be derived from the combined fluctuation of all noise contributions within the VCO loop[6]:

$$\mathcal{L}(f) = \left(\frac{V_{n\max} - \frac{L_{\min} + L_{n1}}{2L_{\min}} V_m}{V_{n\min} - \frac{L_{\min} + L_{n1}}{2L_{\min}} V_m} \right)^2 \left(\frac{I_{n1}^2}{I_{3\max}^2} \right) \left(\frac{K_f}{W_{n1} L_{n1}} + \frac{K_f}{W_{p5} L_{p5}} \right) \left(\frac{f_0^2}{f^3} \right) \quad (9)$$

This improved model gives immediate insight into the mechanisms which impact on the VCO phase noise. Firstly, it is seen that factors which improve phase noise are larger current starved transistors (Mn1, Mp5), more delay stages, a greater supply voltage and a lower value of V_r . Secondly, it is clear that changes in the tuning voltage do result in a change in phase noise performance. When $V_{n\min}$ is increased, the term $V_{inst} - ((L_{\min} + L_{n1})/2L_{\min})V_m$ becomes smaller, leading to an increase in noise level if all other factors stay the same.

3. SIMULATION RESULTS

In order to confirm the accuracy of the proposed phase noise model, a number of example VCOs have been designed. All the transistors in these examples were sized based on equations (1) and (2) and were then simulated using Cadence Spectre and SpectreRF to determine the oscillation frequency and phase noise performance at two control voltages. Table 1 shows the transistor sizing and simulation results. As expected, when the control voltage (V_n) is halved, the oscillation frequency decreases by almost 50%. However, the phase noise does not decrease in the same manner, indeed in some examples, the noise level *increases* by up to 10 dB when the oscillation frequency is halved. By taking the voltage tuning mechanism into account, the novel phase noise model proposed in equation (9) correctly explains these observations.

Figure 3 shows a comparison between the phase noise model and Cadence SpectreRF results over a wide tuning range for each design example. It can be seen that for all the design examples, when the control voltage (V_n) is higher than 0.6V, the errors are no greater than 3dB which confirms the accuracy of the new model. Below 0.6V the cascode transistors (Mn2, Mp2) enter the saturation region of operation and so

the assumptions made in Section 2 are no longer valid.

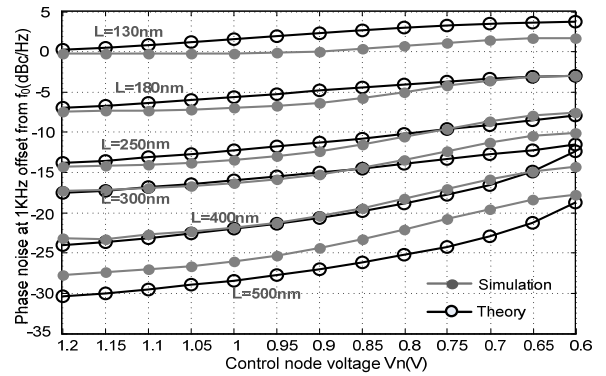


Figure 3 Comparison of simulated and theoretical results

Full layouts have been created for two of the design examples ($L=130\text{nm}/400\text{nm}$) in order to simulate the parasitic capacitances one would expect in practice. These post layout simulation results are shown in Figure 4. As expected, the oscillation frequency has reduced as a result of the extra capacitances. However, when these new oscillation frequencies are used with the model of equation 9, it is found that the theory is still consistent. The noise predicted by existing work is also shown in Figure 4 [6]. Since this does not consider the tuning mechanism then it incorrectly assumes that the noise will decrease with frequency. From simulation this is clearly not the case and results in errors of up to 18dB.

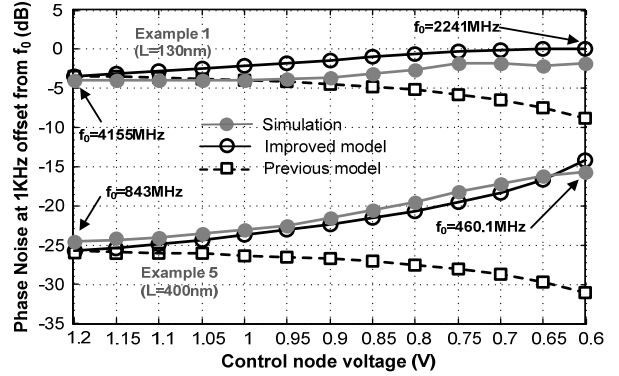


Figure 4 Post layout results from Examples 1 and 5

Table 1 Design examples dimension and performance

Example number:	Transistor Dimensions:		Performance at $V_n=1.2\text{V}$		Performance at $V_n=0.6\text{V}$	
	W_{p5}/L_{p5} (μm)	W_{n1}/L_{n1} (μm)	Oscillation frequency (MHz)	Phase Noise at 1KHz offset from f_0 (dBc/Hz)	Oscillation frequency (MHz)	Phase Noise at 1KHz offset from f_0 (dBc/Hz)
1	103/0.13	40/0.13	6521	-0.237	3592	1.645
2	132/0.18	48/0.18	3934	-7.4	2144	-2.94
3	168/0.25	56/0.25	2301	-14.25	1258	-7.53
4	153/0.3	50/0.3	1695	-17.27	928.8	-10.03
5	202/0.4	64/0.4	1026	-23.21	566	-14.32
6	260/0.5	80/0.5	687.5	-27.72	380.5	-17.77

4. EXTENSION TO SINGLE ENDED VCOS

The theory developed in Section 2 is also valid for the single ended current starved oscillator shown in Figure 5. The only difference in the model is a change in the number of delay stages N , as shown in equation (10). In order to demonstrate the accuracy of the model when applied to single ended structures, a 5 stage single ended ring oscillator was simulated based on the dimensions calculated for design example 5 in Section 3. Figure 6 shows a surface plot of the phase noise against centre frequency and control voltage for both the model in equation (10) and the results obtained from Cadence SpectreRF. Figure 7 shows a contour map indicating the accuracy of the theoretical model for this structure. It can be seen that from 1.2V to 0.7V, the error is less than 0.5dB, which increases to just over 2dB around 0.6V.

$$\mathcal{L}(f) = \left(\frac{V_{n\max} - (L_{nl} + L_{nl})V_m}{2L_{nl}} \right)^2 \left(\frac{I_{nl}^2}{I_{3\max}^2} \right) \left(\frac{K_f}{W_{nl}L_{nl}} + \frac{K_f}{W_{p5}L_{p5}} \right) \left(\frac{f_0^2}{f^3} \right) \quad (10)$$

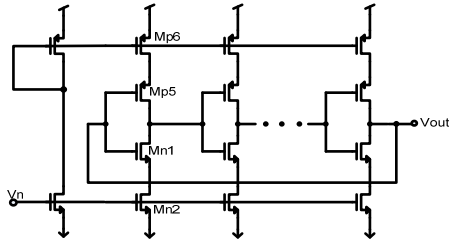


Figure 5 Single ended current starved oscillator

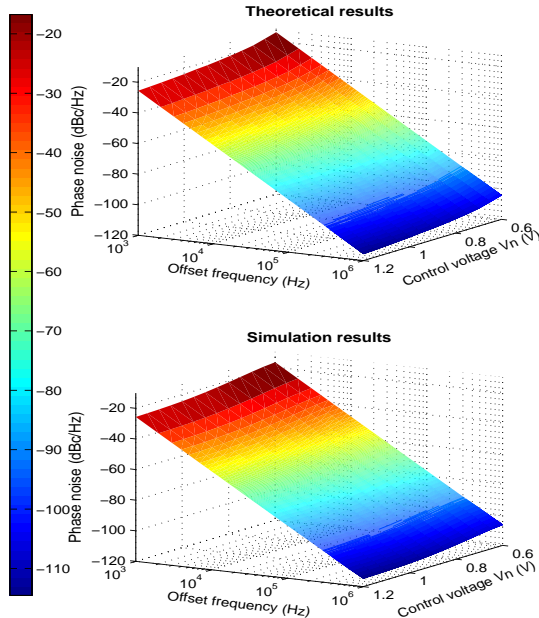


Figure 6 Noise results for singled ended design examples

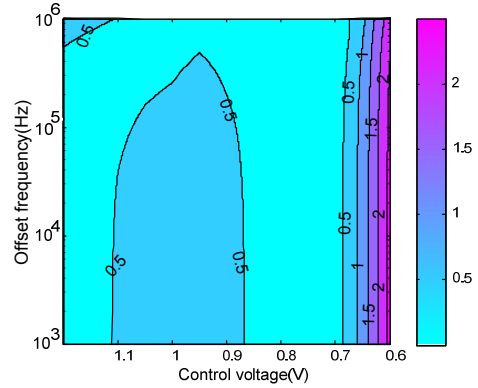


Figure 7 Accuracy analysis for single ended design examples

5. CONCLUSIONS

Many models already exist to predict the phase noise from VCOs, but they only model the noise performance at one oscillation frequency. In wide band VCOs, it is important to model phase noise performance over the majority of the tuning range, to give greater insight into the mechanisms involved. This work has proved that the tuning voltage of a VCO does impact on the phase noise performance and has explained the cause of this impact. An improved phase noise model has been proposed which models the phase noise performance of an ultra wideband differential VCO over the majority of its tuning range. A wide range of design examples have been presented to validate the theoretical model which has also been extended to single ended designs. Simulating noise in conventional tools can take hours for even a simple measurement, and so the model proposed in this paper gives a significant advantage to designers.

6. REFERENCES

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