

2010 IEEE International Behavioral Modeling and Simulation Conference  
Modeling for Physical Design Session

# Automatic Stress Effects Computation Based On A Layout Generation Tool For Analog IC

**Stephanie YOUSSEF**

Damien DUPUIS

Ramy ISKANDER

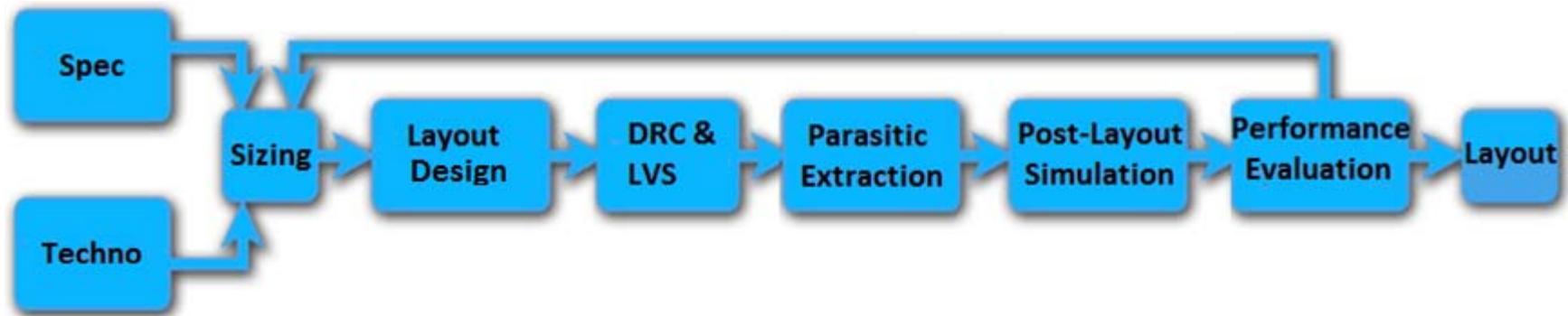
Marie-Minerve LOUERAT

LIP6 Laboratory, Université Pierre et Marie-Curie, Paris, France

# Plan

- Introduction :
  - a. Problem definition
  - b. Proposed design flow
- Stress effect modeling  
for CMOS transistors devices
- Results
- Conclusion

## Traditional design Flow



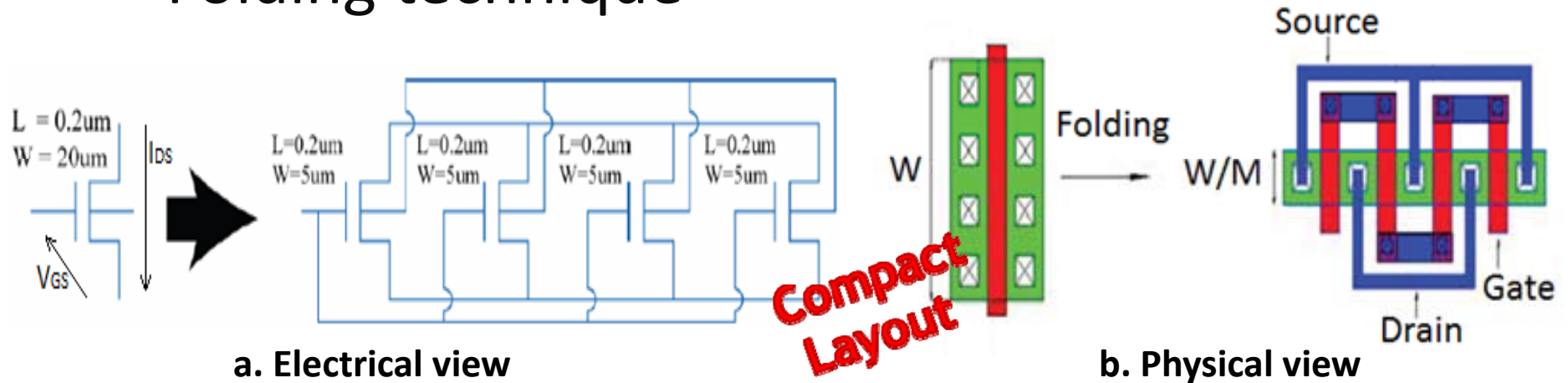
### Description:

- An iterative process
- Manual design Flow
- High number of iterations
- Several steps supported by different tools

### Disadvantages:

- Time Consuming
- Subject to human errors

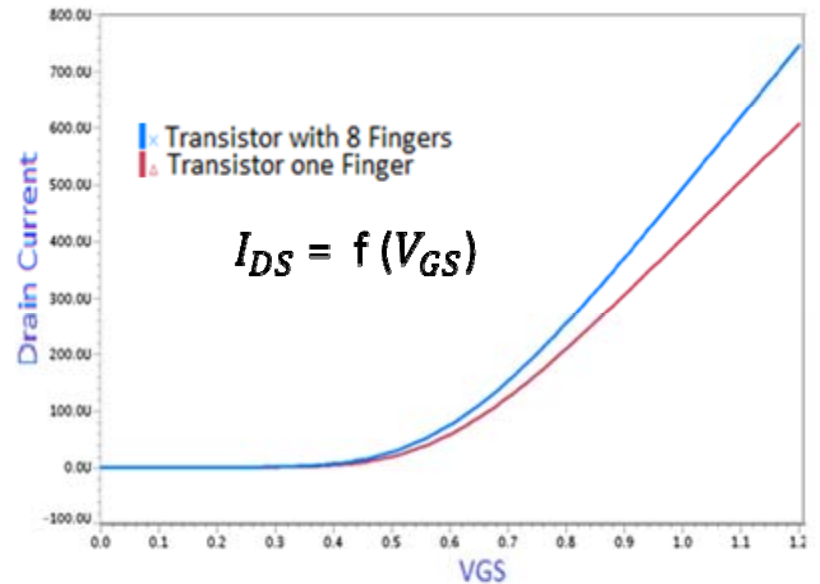
■ Folding technique



$$I_{DS} = \mu C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2$$

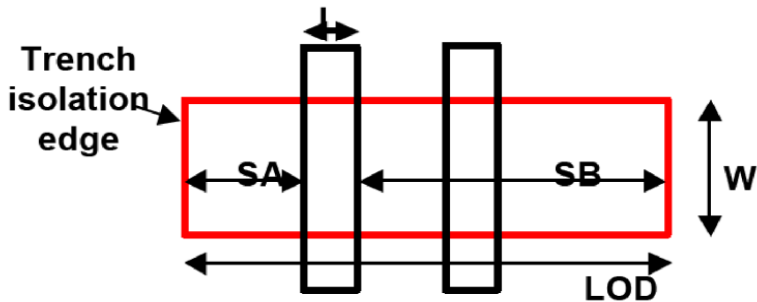
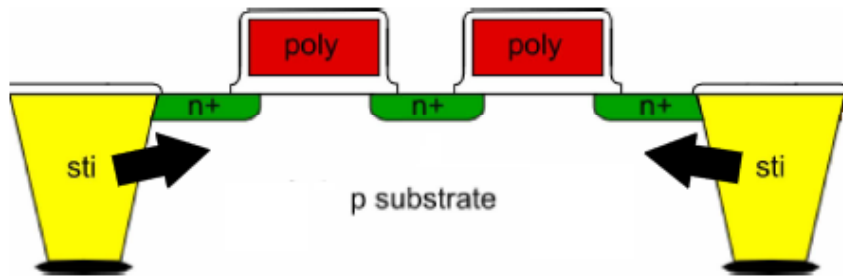
$$I_{DS}(W_{Total}) \neq M \times I_{DS}\left(\frac{W_{Total}}{M}\right)$$

- Parasitic capacitance ↓ and gate resistance ↓
- Inverse narrow width effect:  
Wf ↓, Doping ↓, Vth ↓ so IDS ↑
- Aligned W to be on the physical grid



Strong link between  
Layout and performance!

■ STI (Shallow Trench Isolation)



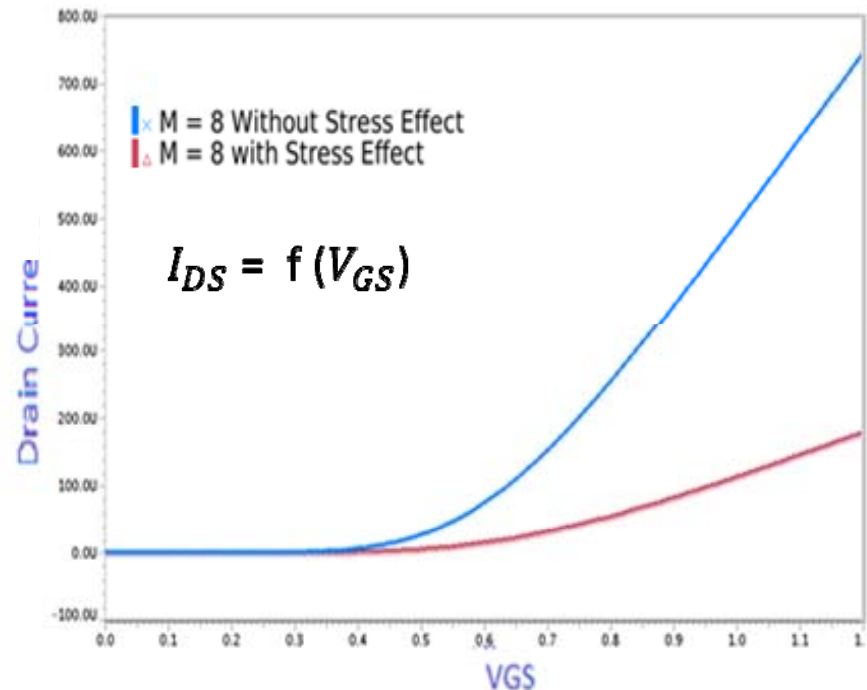
$LOD = SA + SB + L$     OD: gate Oxide Definition

$$\mu_{eff} = \frac{1 + \rho \mu_{eff}(S_a + S_b)}{1 + \rho \mu_{eff}(S_{areff} + S_{breff})} \mu_{eff0}$$

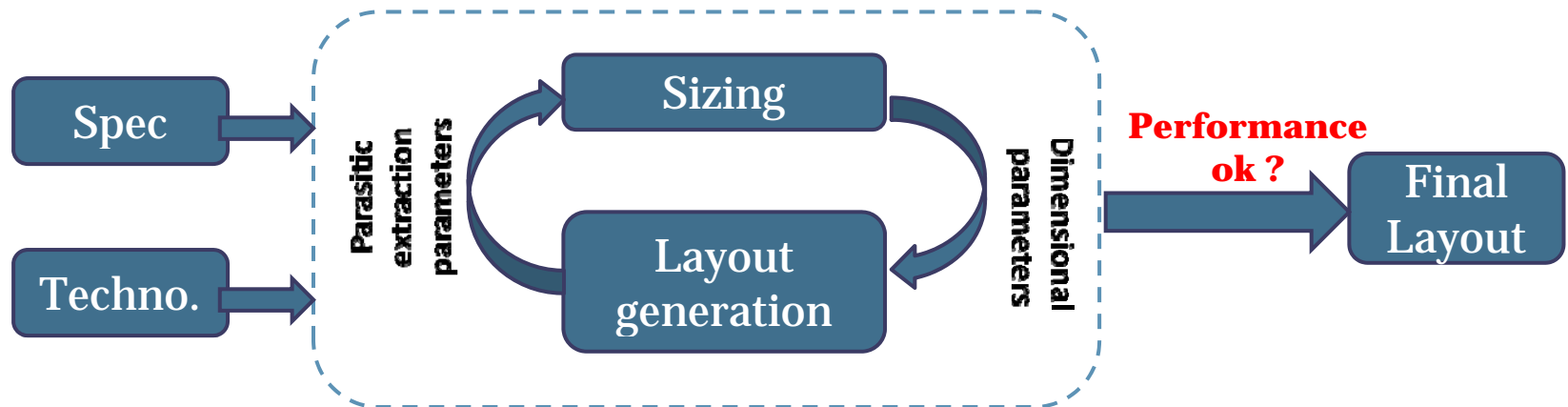
$$V_{sat} = \frac{1 + K \cdot \rho \mu_{eff}(S_a + S_b)}{1 + K \cdot \rho \mu_{eff}(S_{areff} + S_{breff})} V_{sat0}$$

Too complicated for design using the traditional flow !

- Isolation for nanometric technologies
- Latchup protection
- Induces mechanical stress
- Effect on  $\mu_{eff}, V_{sat}, V_{th}$  and  $I_{DS}$
- BSIM4 model



## Proposed design flow



### Goals :

- Speed up the design flow.
- Minimize possible errors.
- Provide a two ways communication between the sizing and layout generation.
- Strongly coupling between layout and sizing

### Internal Loop:

- Repeated several times.
- With minimal designer intervention.

- Contributions of the proposed design flow
  - ✓ Supports fast and accurate methods for parasitic calculations.
  - ✓ Supports different layout styles for each device.
  - ✓ Layout portable over different technologies.
  - ✓ Supports Python description for the layout (ease of the modifications for the layout code).
- ➡ Provides a Customizable, Deformable and Reusable Layout.

## ■ Stack Object

- Goal = Deformable and reusable layout .
- Python code.
- *createStack(*

**Type** = type of the transistor NMOS or PMOS -> **NMOS**,

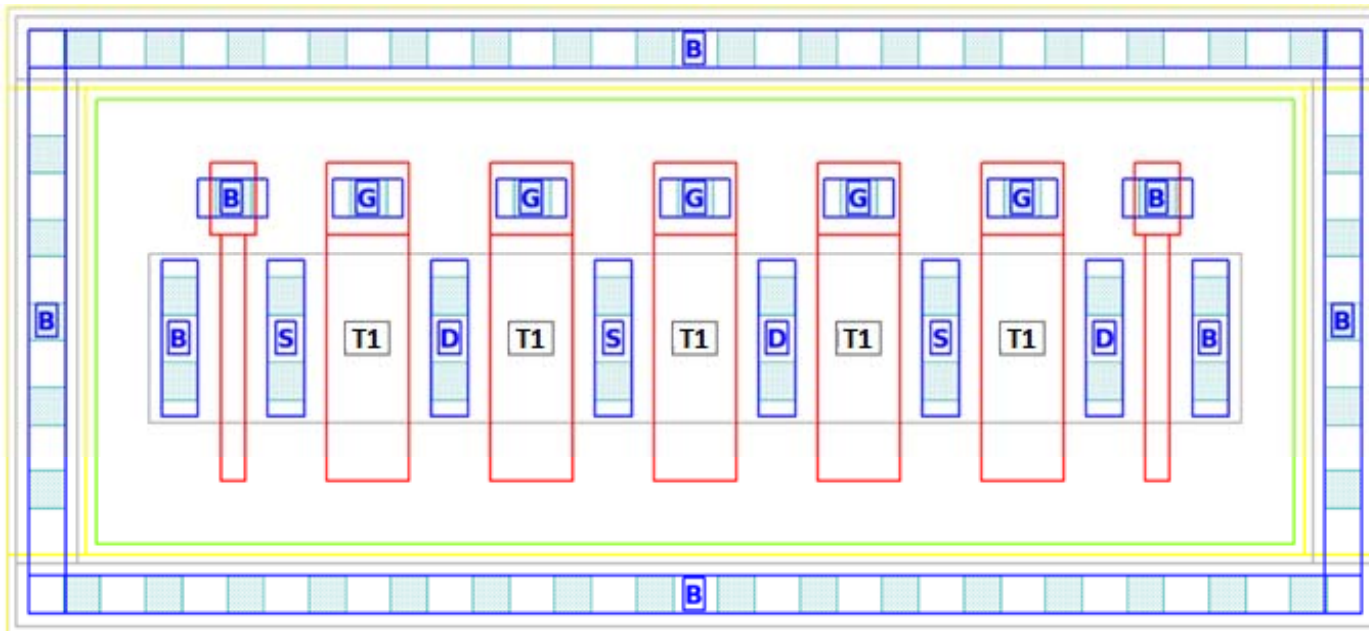
**W** = The overall width of the transistor -> **2  $\mu$ .m.** ,

**L** = The length of each finger (except dummies) -> **0.15  $\mu$ .m.** ,

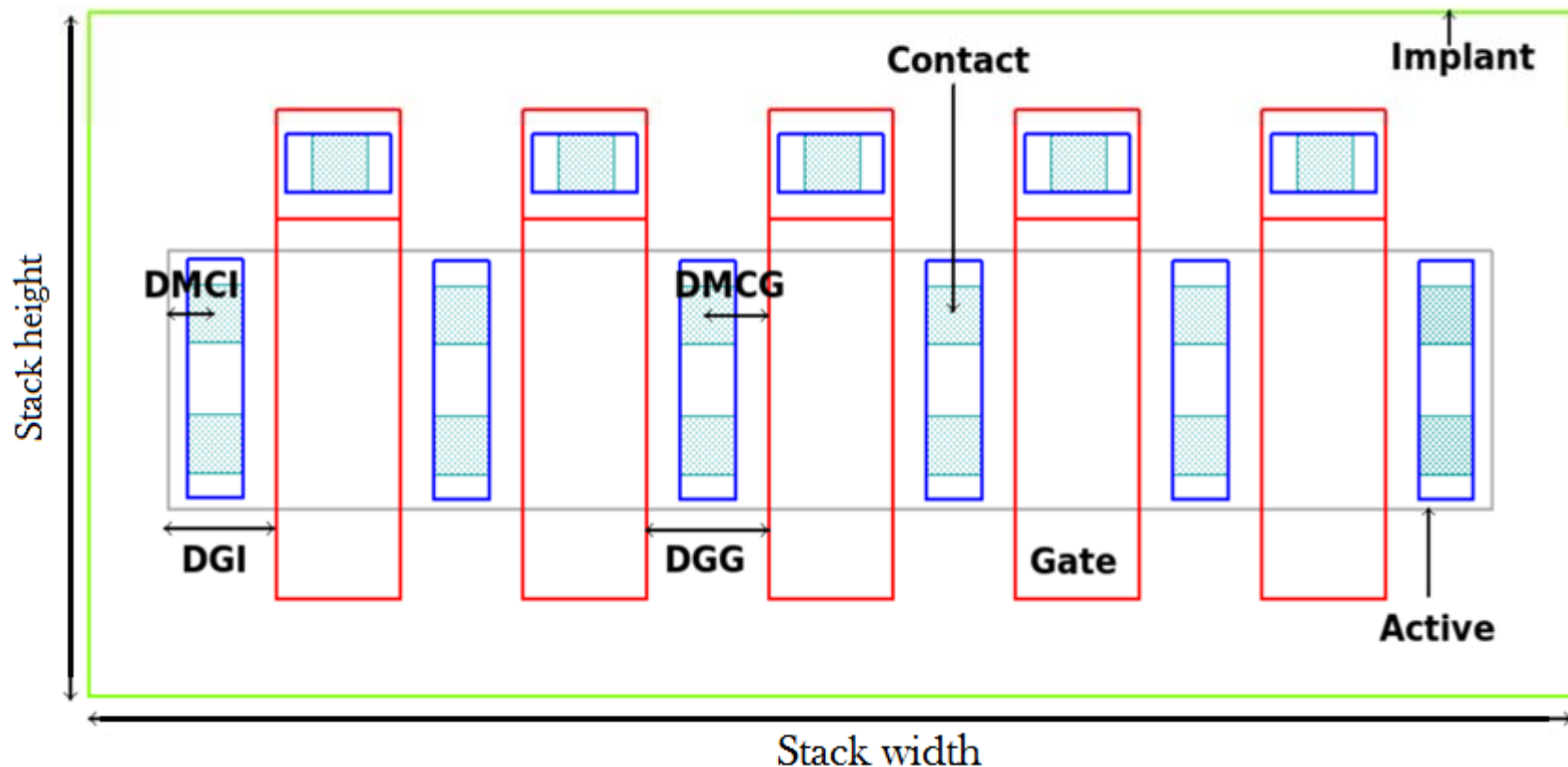
**NFS** = The number of stack's fingers (including dummies) -> **7**,

**NbDummies** = The number of dummies at each stack's end -> **1**

Example : 65 n.m technology and BSIM4 model :

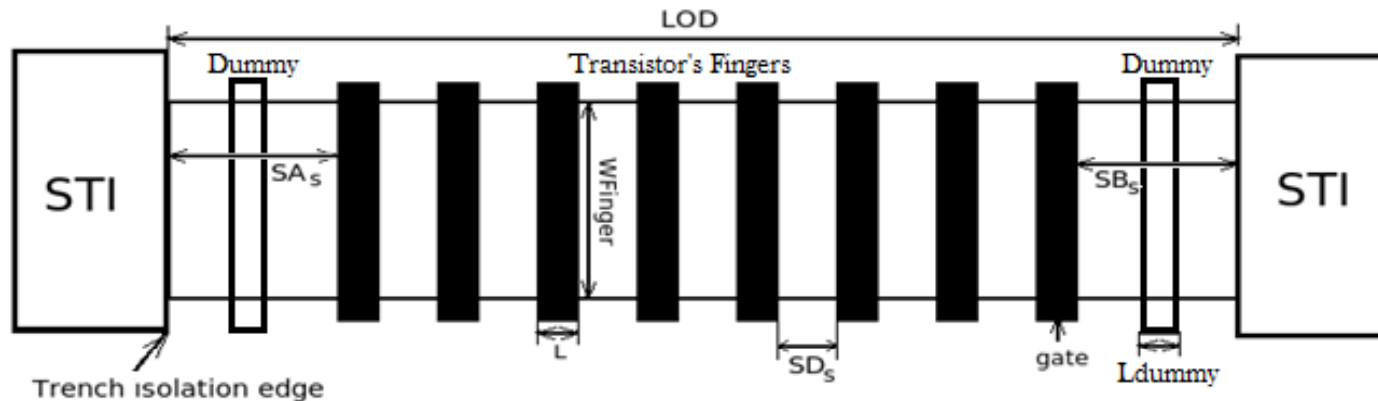


- Distance values provided by the stack object



- STI parameters such as SA and SB depends on (DMCI, DGI, DGG)
- Mismatch(DMCI, DMCG, ...)
- Can add any other geometrical distances information

- Stress effect computation



Considering a stack "S"

### Definitions:

**SA<sub>s</sub>** : Distance gate edge at the left end till the isolation edge at the left end

$$SA_s = DGI + NB_{dummies} \times (L_{dummy} + DGG)$$

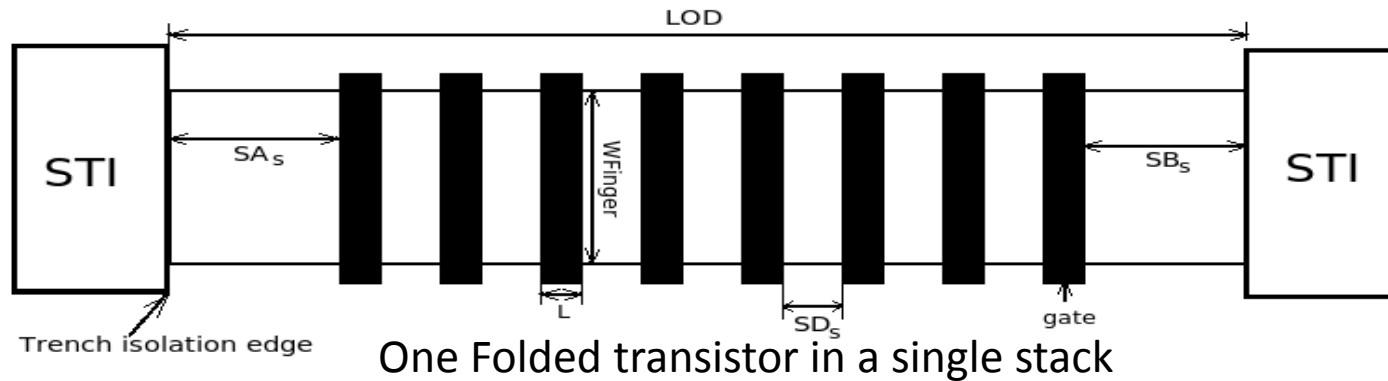
**SB<sub>s</sub>** : Distance gate edge at the right end till the isolation edge at the right end

$$SB_s = DGI + NB_{dummies} \times (L_{dummy} + DGG)$$

**SD<sub>s</sub>** : Distance between two successive gates

$$SD_s = DGG$$

- BSIM4 model : Transistor stress effects



$$Inv_{SA} = \sum_{i=0}^{NF-1} \frac{1}{SA_s + 0.5L_{drawn} + i.(SD_s + L_{drawn})}$$

$$Inv_{SB} = \sum_{i=0}^{NF-1} \frac{1}{SB_s + 0.5L_{drawn} + i.(SD_s + L_{drawn})}$$

$$SA_{eff} = \frac{1}{Inv_{SA}}, SB_{eff} = \frac{1}{Inv_{SB}}$$

$$\frac{1}{\alpha} = \frac{1}{2.SA_{eff}} + \frac{1}{2.SB_{eff}}$$

$\mu_{eff}$  and  $V_{sat}$  depend on  $(SA_{eff}, SB_{eff})$

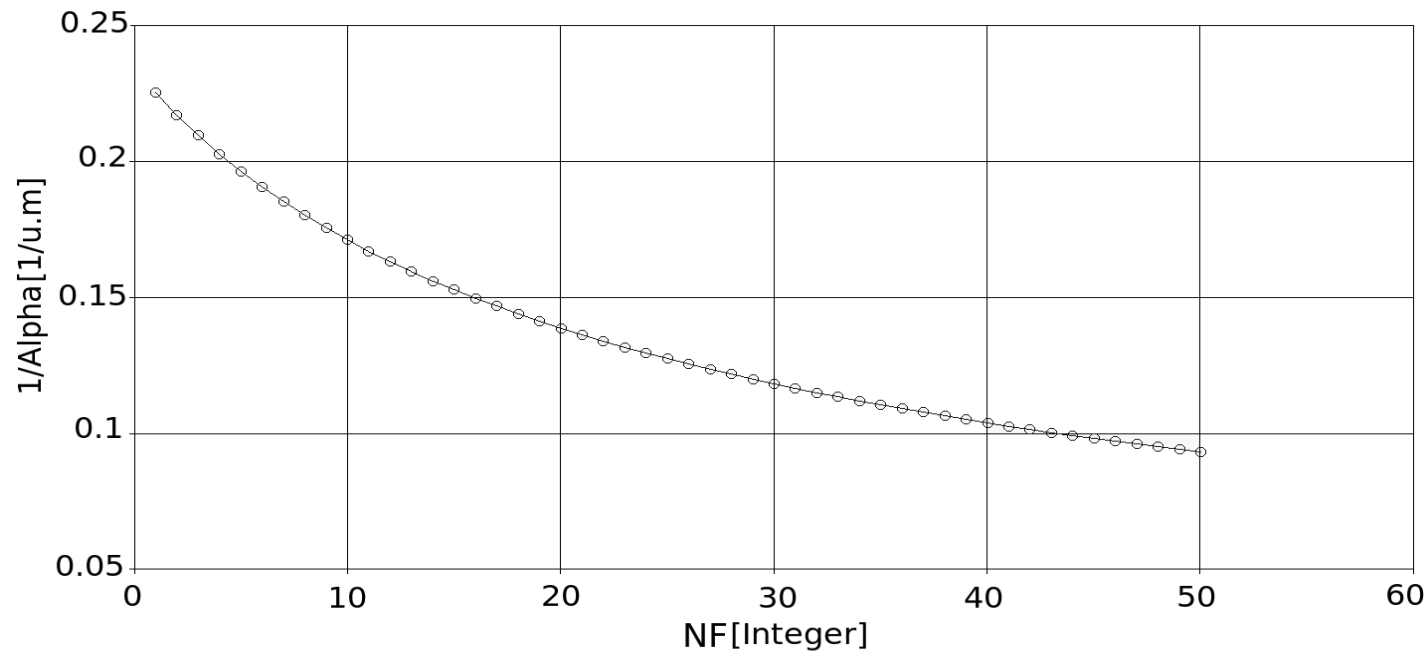
$Inv_{SA}, Inv_{SB} \downarrow$

$\frac{1}{\alpha} \downarrow$

**Stress**  $\downarrow$

## ■ Automatically generated curves

Technology = 65 nm , W= 6  $\mu\text{m}$  and L = 0.15  $\mu\text{m}$



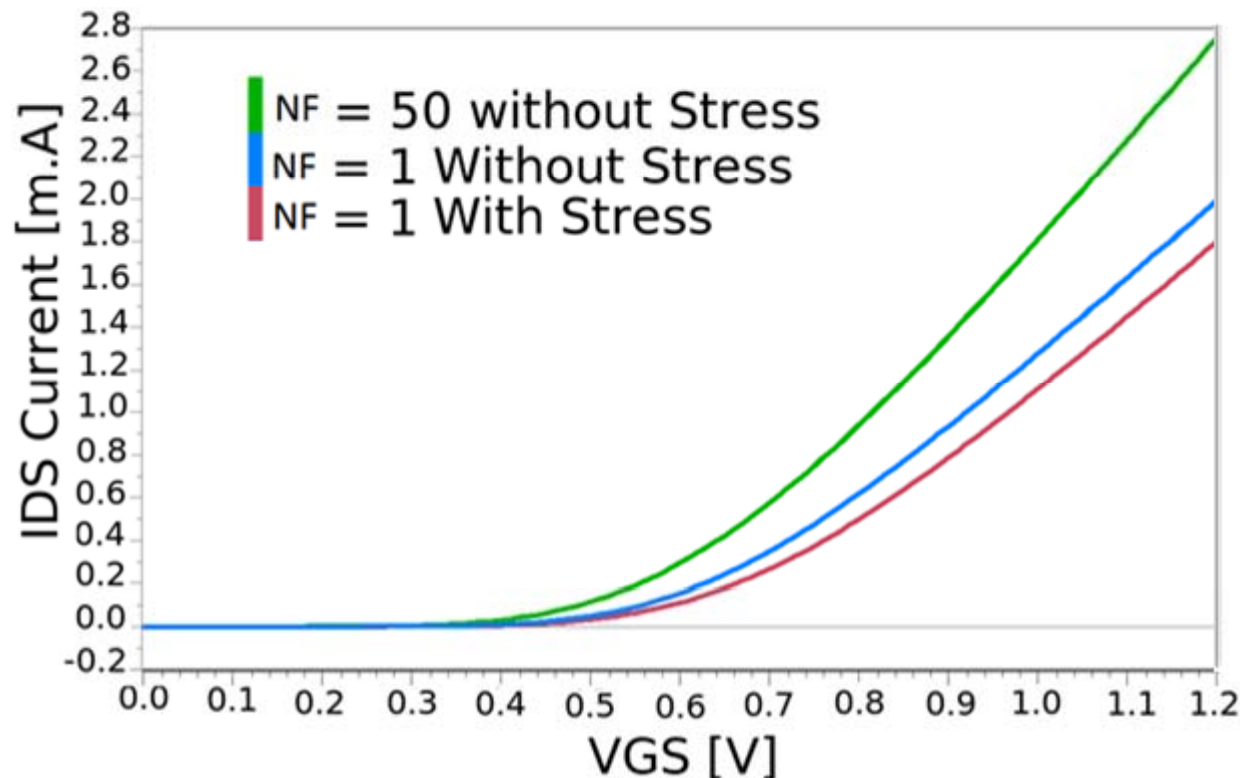
One Folded transistor in a single stack

- **Effective stress effect directly proportional to  $\frac{1}{\alpha}$**
- **Taking the advantage of the stack object to study the layout parameters**
- **We must study the folding effect**

- Stress and folding effects impact on current

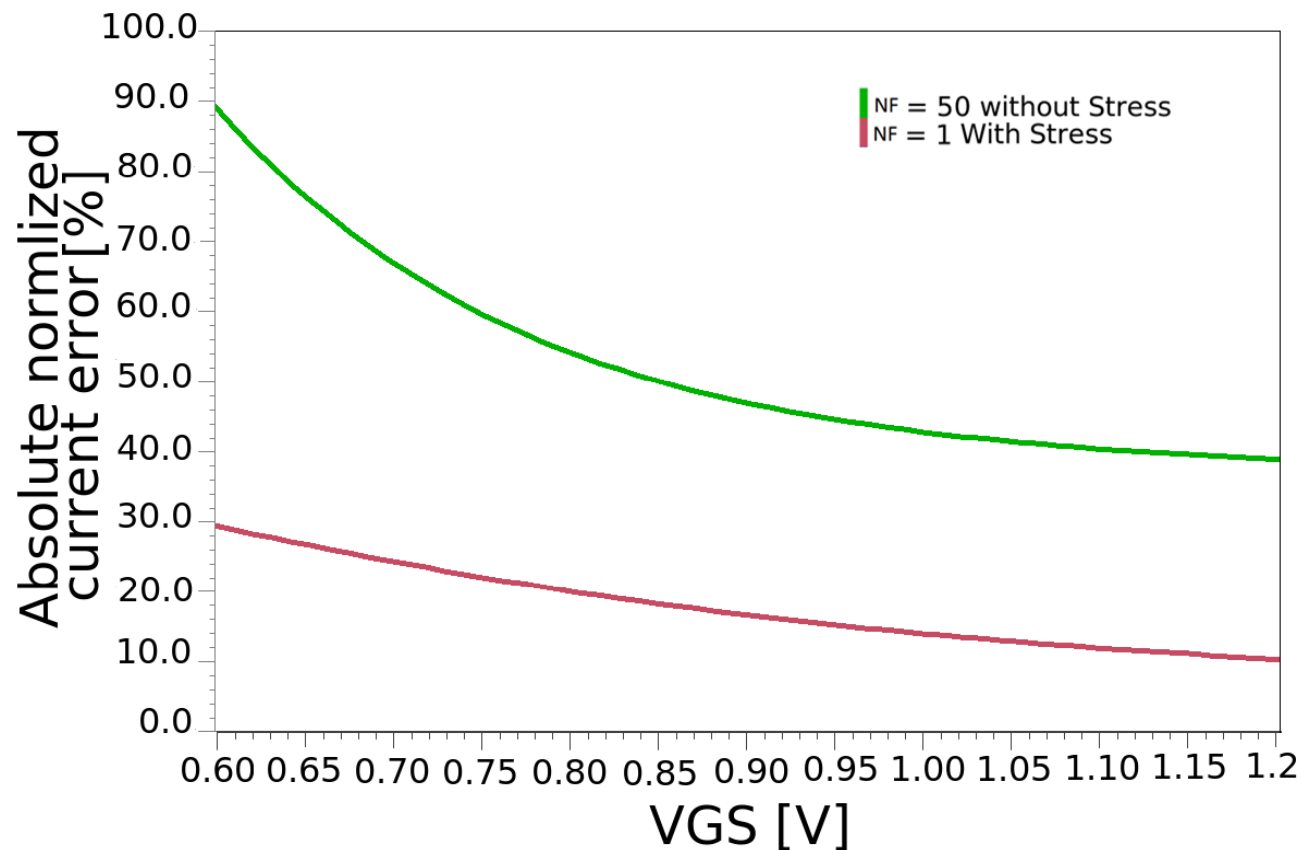
For a same large  $W = 6 \mu\text{m}$  and  $L = 0.15 \mu\text{m}$ :

1. Stress : NF = 1 with stress effects -> Maximum effect  
NF = 1 without stress effects
2. Folding: NF = 50 for a large range  
NF = 1 without stress effects



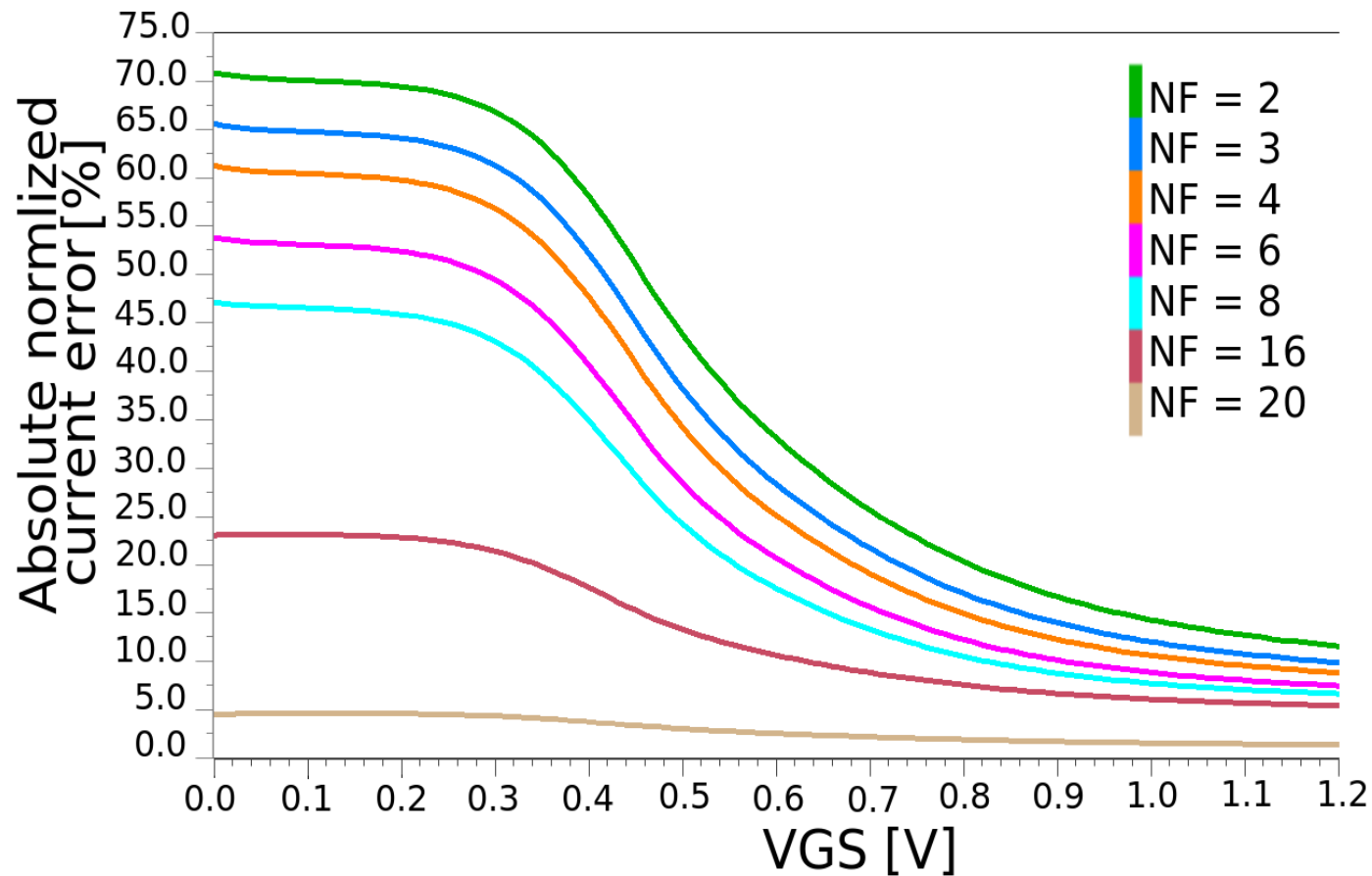
- Comparison between stress and folding effects

$$Error = 100 \times \left| \frac{IDS - IDS_{Ref}}{IDS_{Ref}} \right|, \quad IDS_{Ref} \text{ case when } NF = 1 \text{ without stress}$$



**We must take into consideration the two effects!**

- Reducing the stress effects by increasing NF



NF ↑

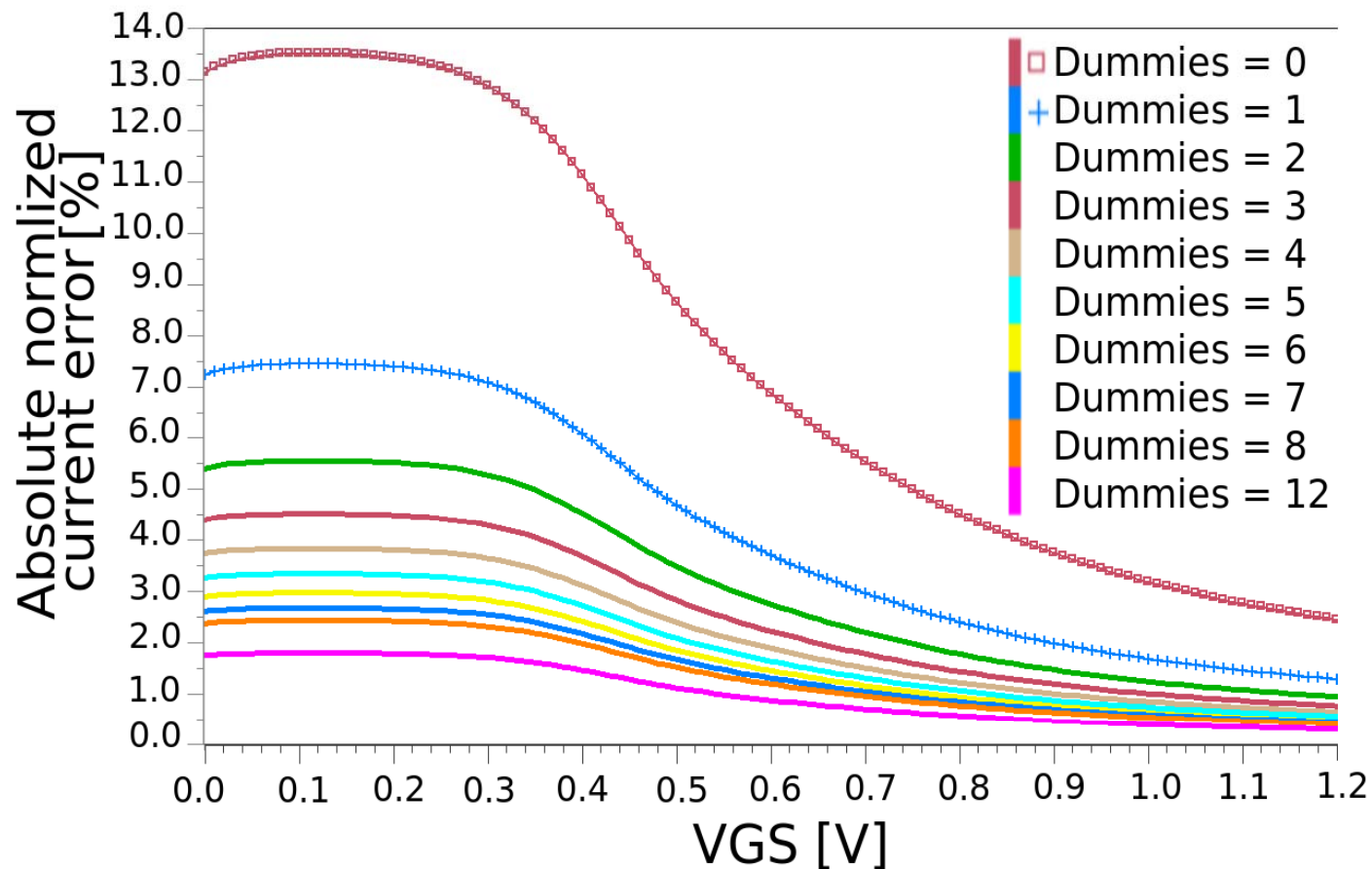
Folding ↑

(SA\_eff and SB\_eff) ↑

Stress ↓

Error ↓

## Reducing the stress effects by adding dummies



Number of dummies ↑

Folding =

Stress ↓

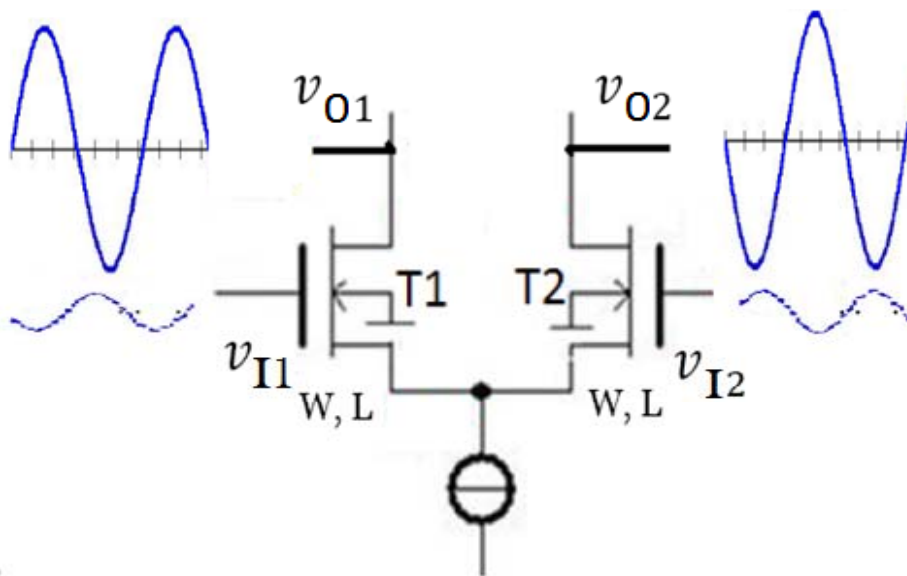
Error ↓

Surface ↑



Tradeoff between performance and surface !

- Mismatch problem between two transistors  
Differential pair example:



$$v_{O1} = V_{O1} + v_{o1}$$

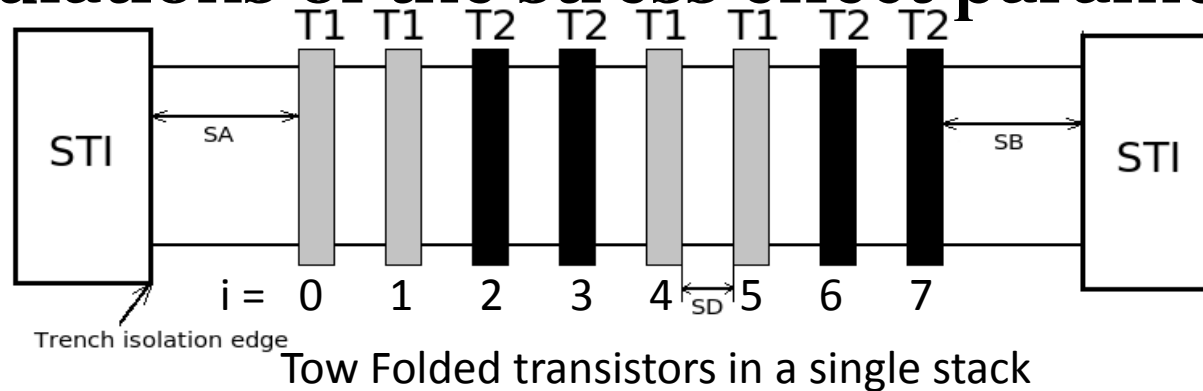
$$v_{odiff} = v_{O1} - v_{O2}$$

$$v_{odiff} = V_{O1} + v_{o1} - V_{O2} + v_{o2}$$

$$v_{odiff} = v_{o1} - v_{o2}$$

➡ Dedicated Layout Styles to reduce the mismatch !

■ Calculations of the stress effect parameters



if  $Finger_i \in T1$ :  $i \in \{0,..,7\}$  : Finger index  
 $\delta_{i,j} = 1$   $j \in \{1,2\}$  : Transistor index  
 Else :  
 $\delta_{i,j} = 0$

$$(Inv_{SA})_j = \sum_{i=0}^{NFS-1} \frac{\delta_{i,j}}{SA_S + 0.5L_{drawn} + i.(SD_S + L_{drawn})}$$

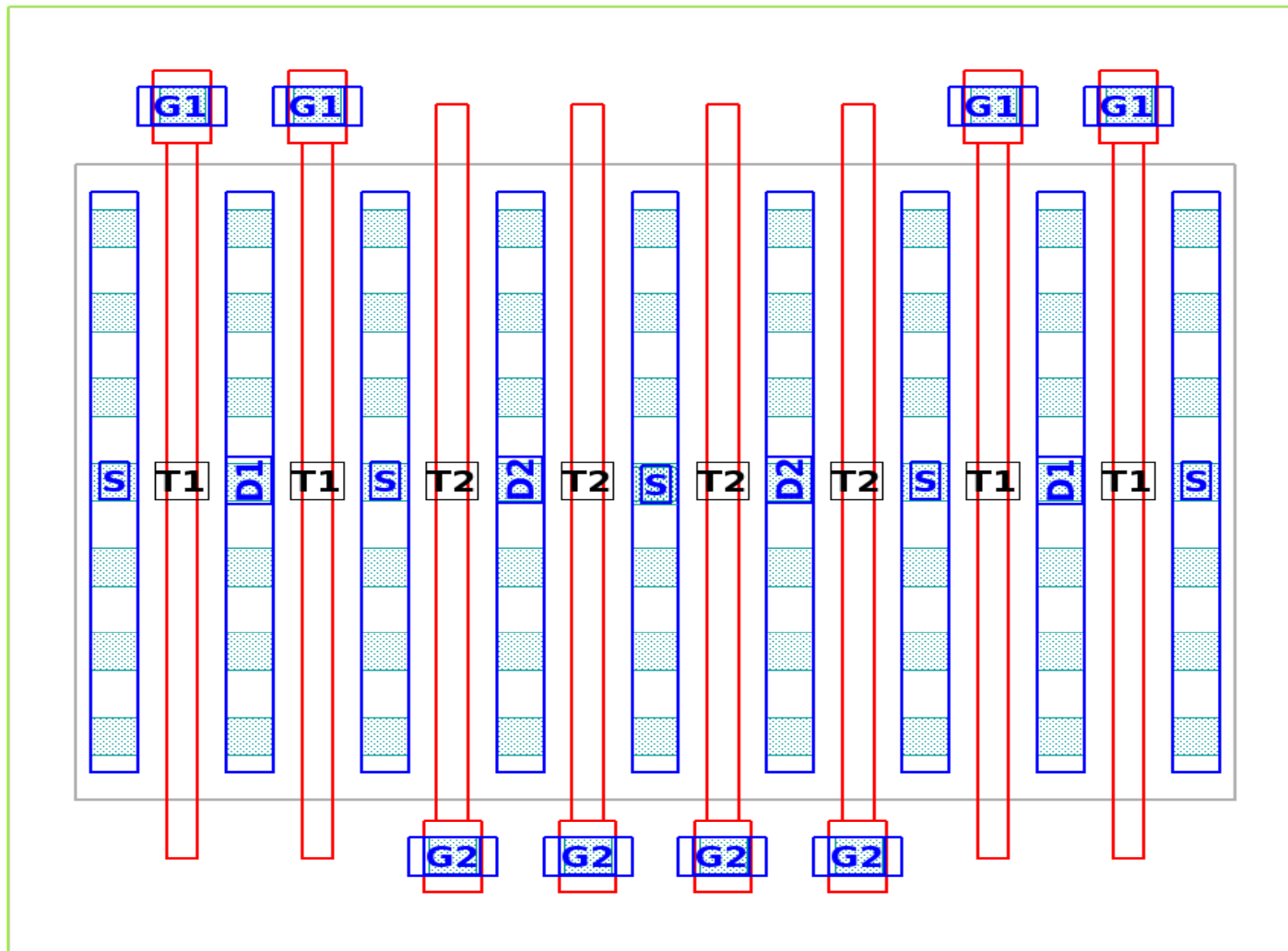
$$(Inv_{SB})_j = \sum_{i=0}^{NFS-1} \frac{\delta_{i,j}}{SB_S + 0.5L_{drawn} + i.(SD_S + L_{drawn})}$$

$$(SA_{eff})_j = \frac{1}{(Inv_{SA})_j}, (SB_{eff})_j = \frac{1}{(Inv_{SB})_j}$$

$$\frac{1}{\alpha_j} = \frac{1}{2(SA_{eff})_j} + \frac{1}{2(SB_{eff})_j}$$

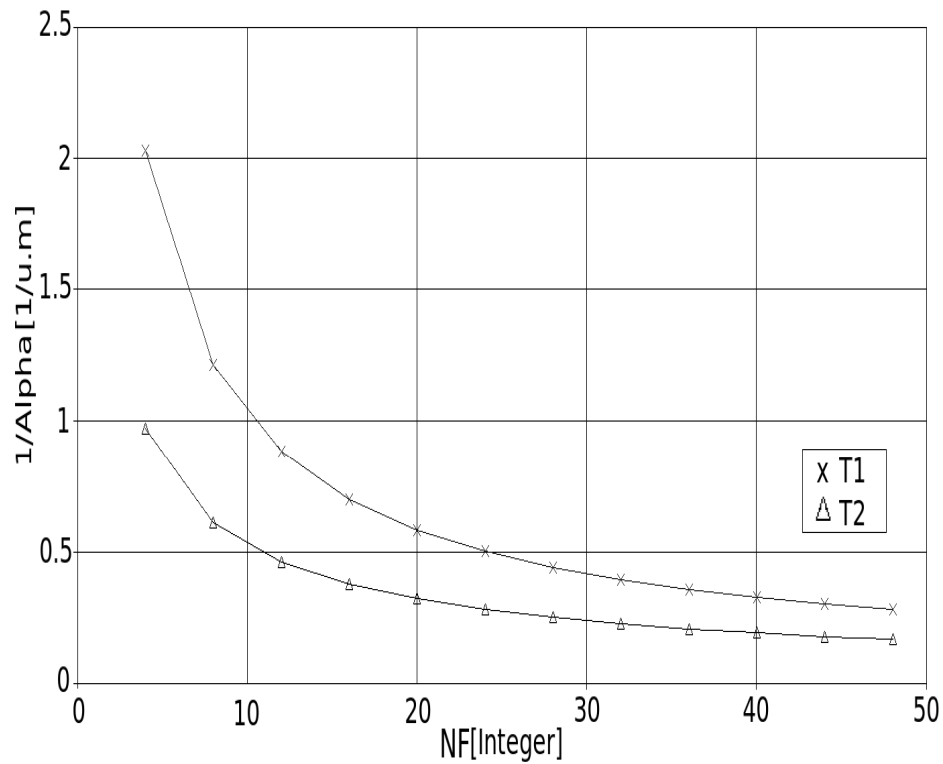
- Differential Pair symmetrical style

Technology = 65 nm , W= 6  $\mu\text{m}$  and L = 0.06  $\mu\text{m}$ , NF = 4

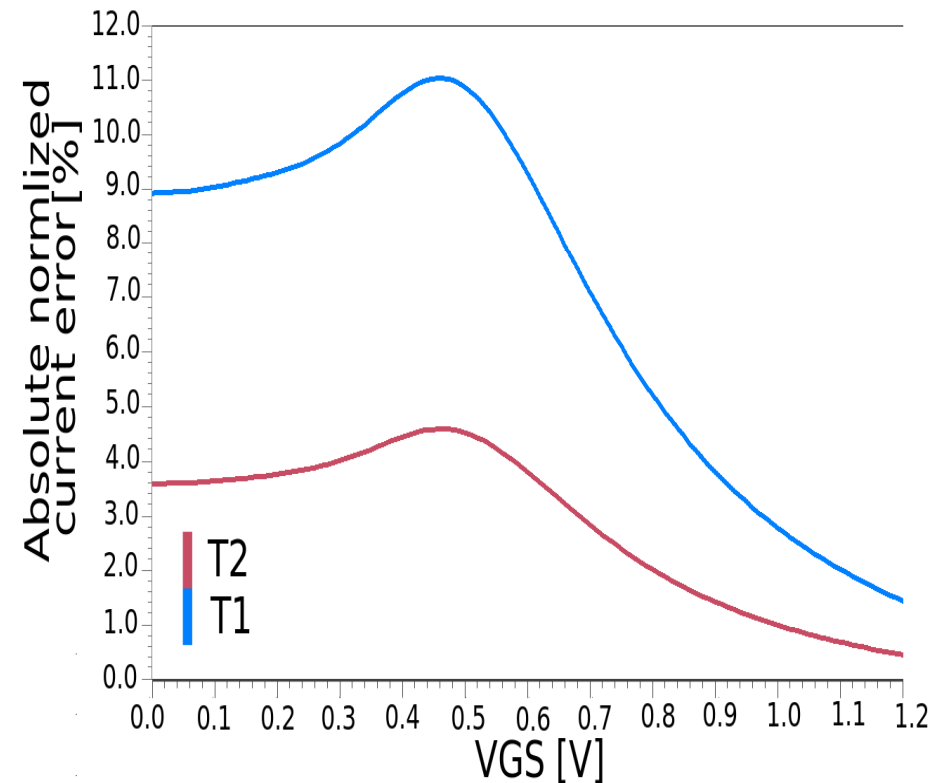


## ■ Differential Pair symmetrical style

**Results:**  $IDS_{Ref}$  case when  $NF = 4$  without stress



a.  $(1/\alpha)$  v.s NF generation curves



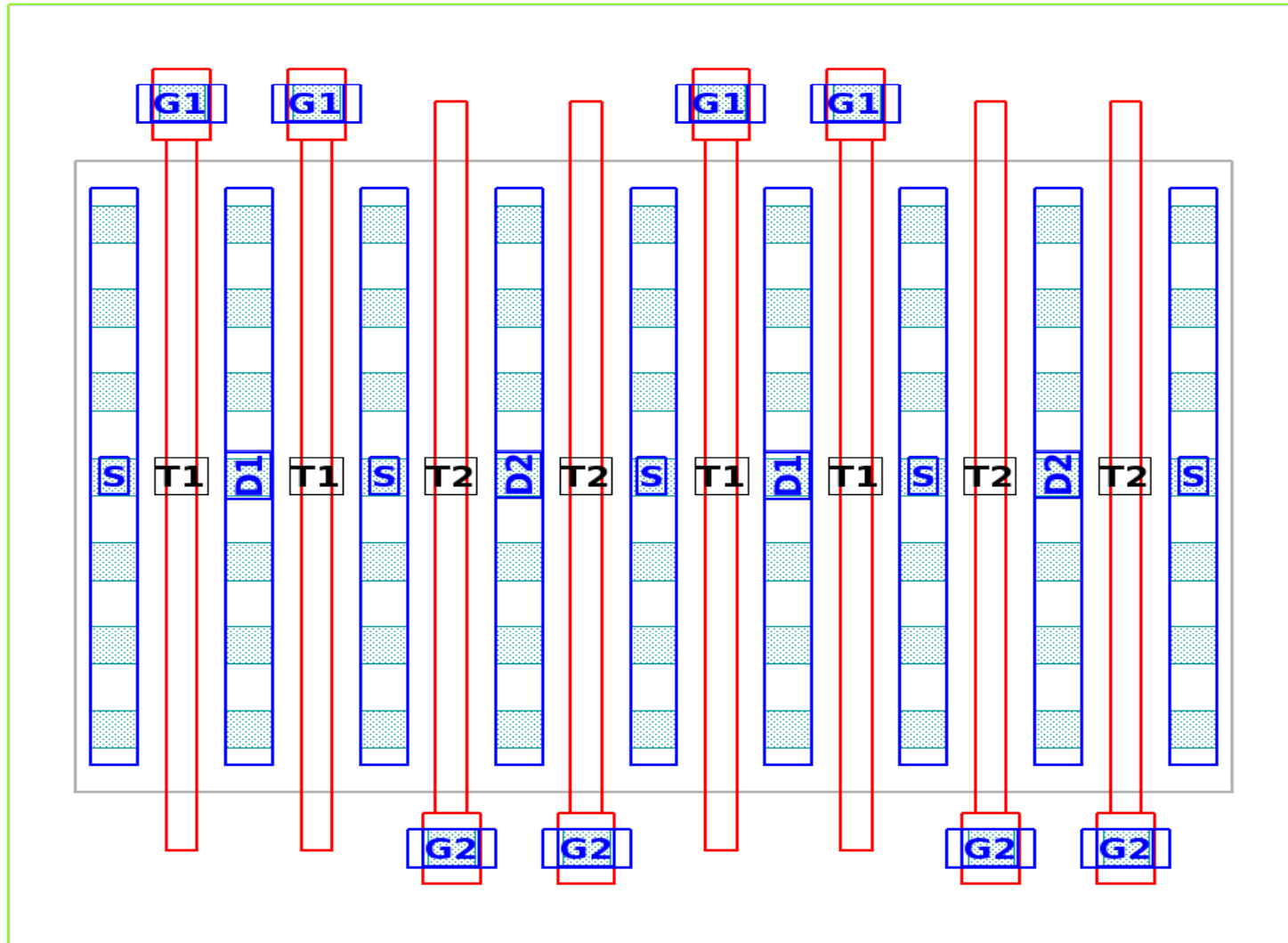
b. Current error simulation curves



Different stress and error for the two transistors!

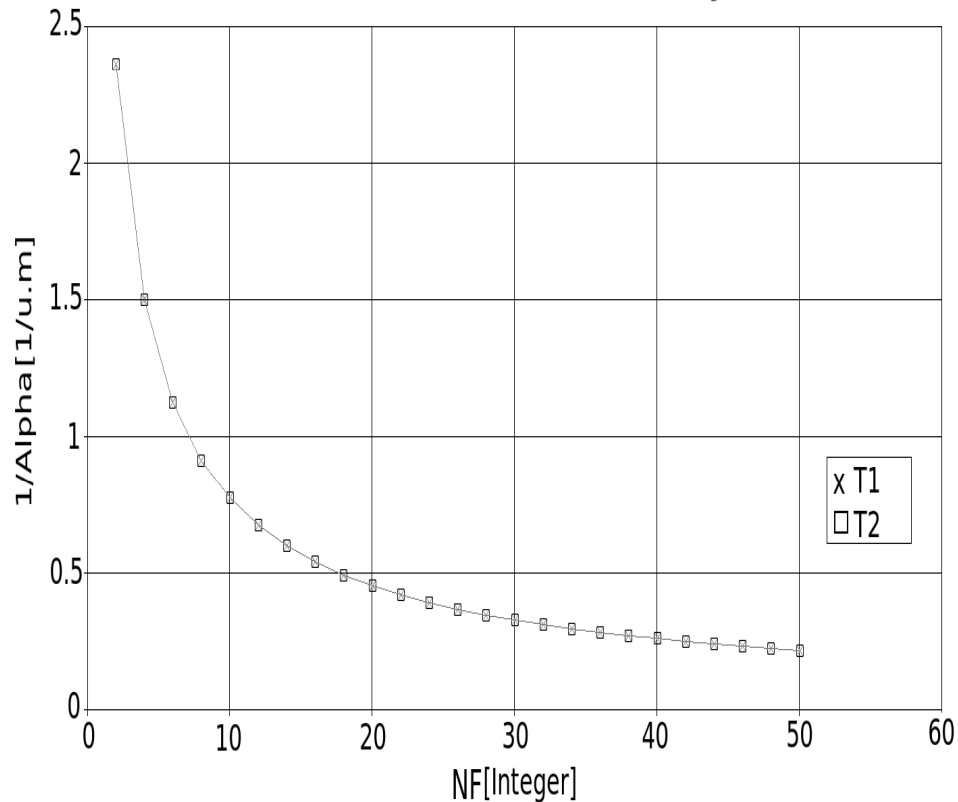
- Differential Pair interdigitated style

Technology = 65 nm ,  $W = 6 \mu\text{m}$  and  $L = 0.06 \mu\text{m}$ ,  $NF = 4$

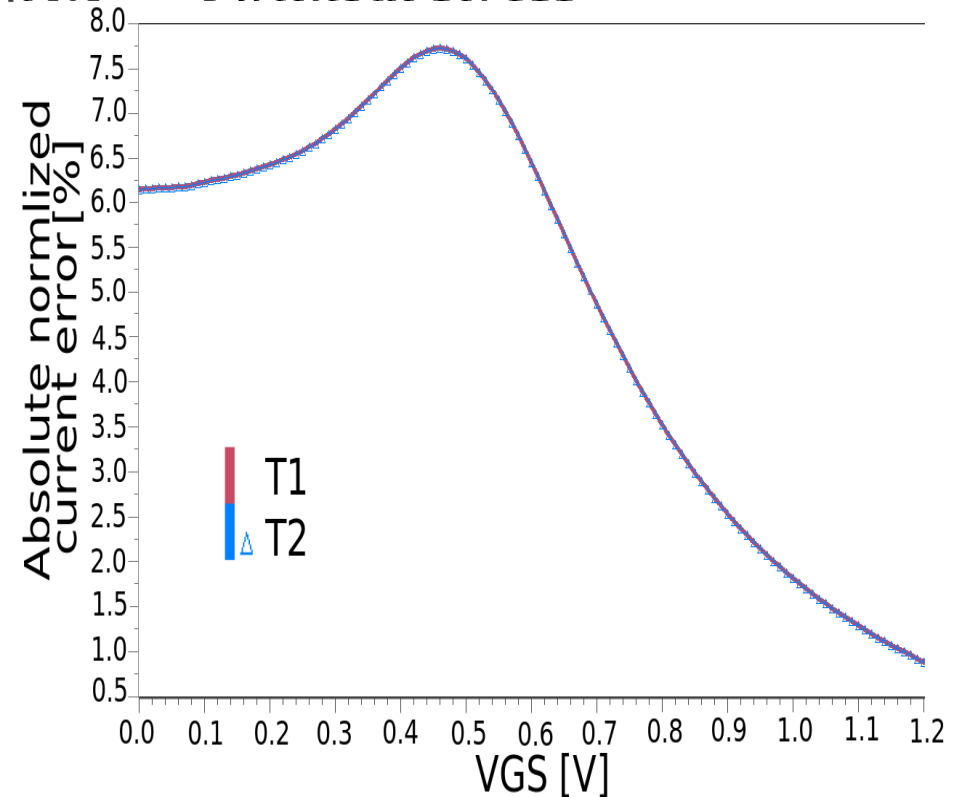


## ■ Differential Pair Interdigitated style

Results :  $IDS_{Ref}$  case when  $NF = 4$  without stress



a.  $(1/\alpha)$  v.s NF generation curves



b. Current error simulation curves

➡ Same stress and error for the two transistors!

**In nanometer technologies Interdigitated style is preferred !**

# Conclusion

- We proposed a design flow to generate layouts for nanometers devices
- A Python API has been extended to compute stress effects
- Combined effects of stress and folding have been investigated
- The proposed flow has been successfully used to characterize different layout styles
- Show that the technology impact on the layout style choice
- Future work will focus on creating portable devices and integrating more nanometer effects