EMI Modeling of a 32-bit Microcontroller in Wait Mode

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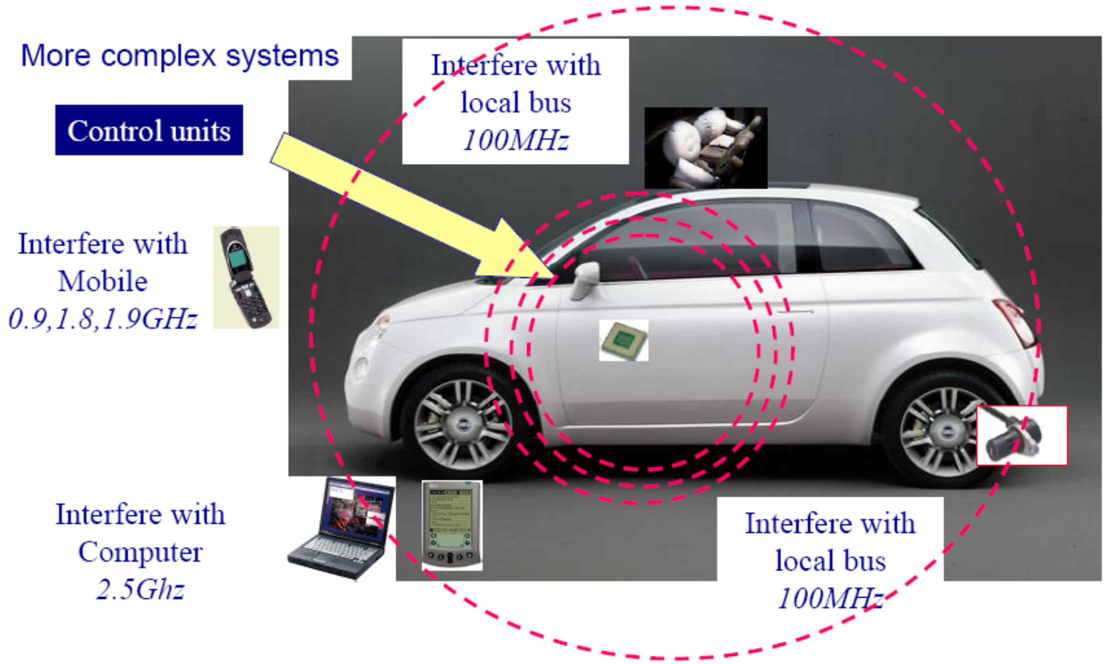
Outline

1. Motivations
2. EMI Background
3. EMI Modeling
4. Results and correlation
5. Conclusion

1. Motivations

EMI: Disturbances that affect an electrical circuit due to either EM conductior … rce.

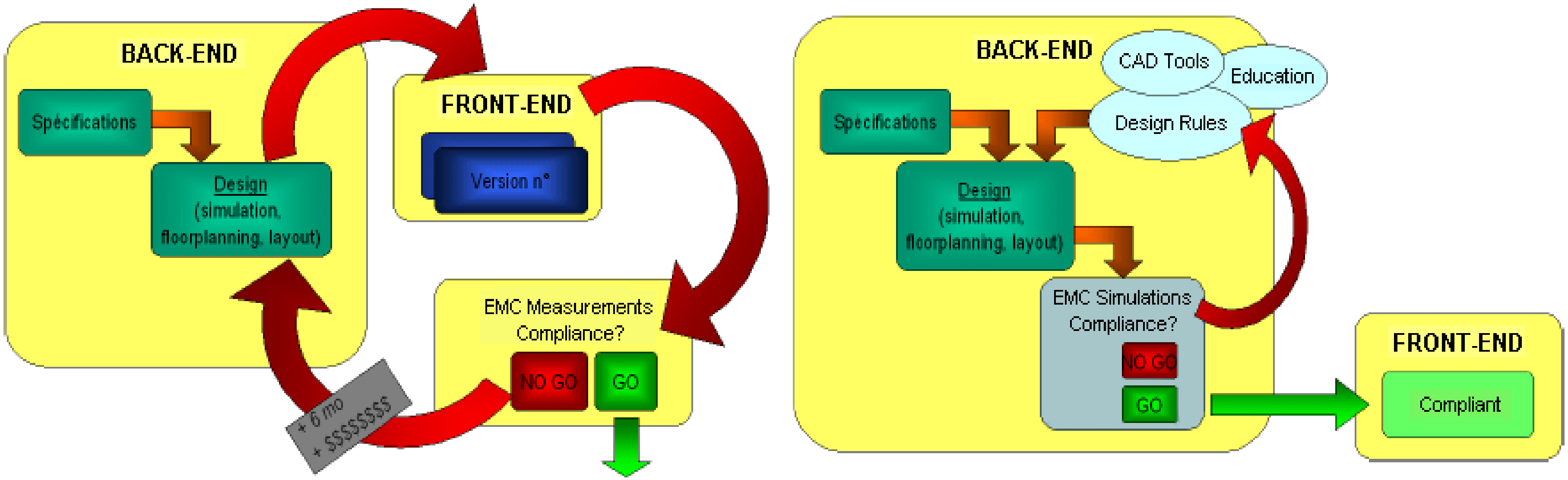


Why?

- EMI are generally increasing with the shrink of CMOS technology & the rise of products' performances.
- Products must be IEC 61967-2 or SAE J1752/3 compliant.
- Marketing argument (automotive, medical, GPS…).
- To save time, money, and gain market share.

1. Motivations

How?



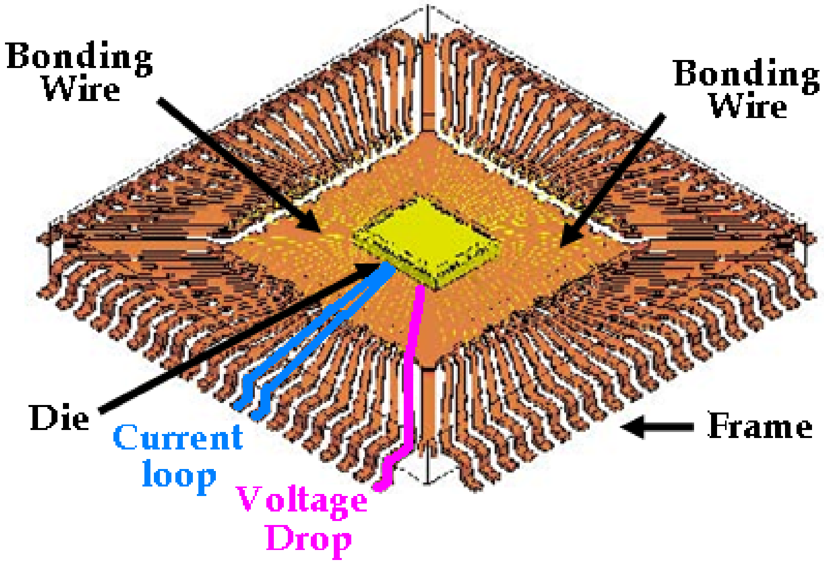
- Before we were expected, now we want to act.

- Define EMI strategy during the design stages by:
  - ❑ Use of predictive EMI models.
  - ❑ Layout/Design rules implementations during the product design flow.

2. Background

Basic EMI mechanisms:

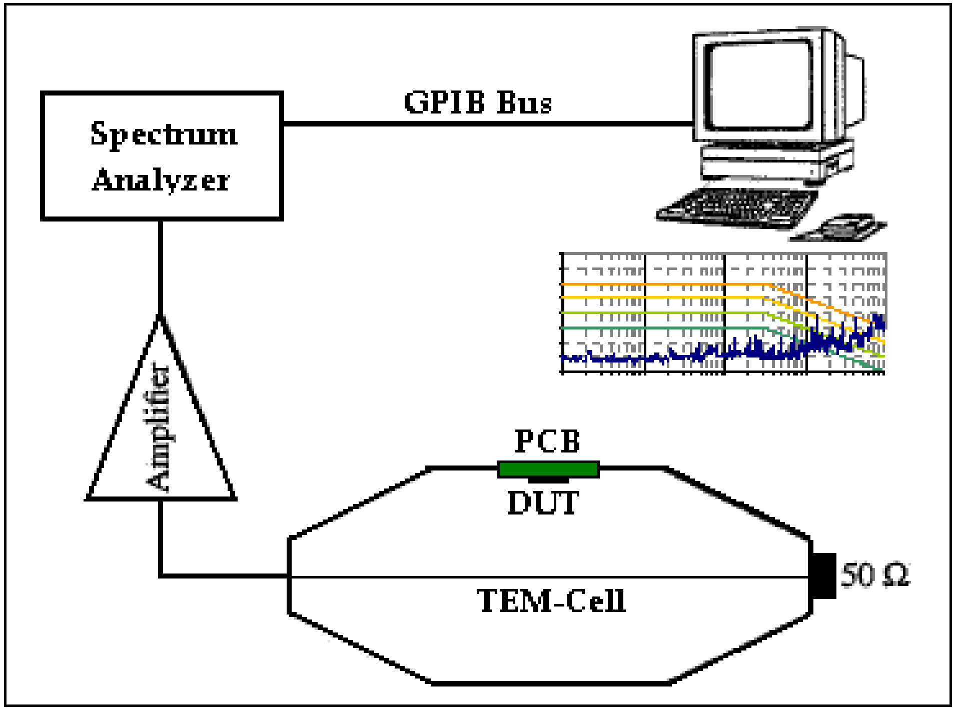
- Noise generation due to switching currents created by:
  - ❑ Clock-driven blocks, synchronized digital core
  - ❑ Accesses to the memories (Flash, RAMs, …), I/O switching activity
- AC currents converted into P/G voltage drops (common mode radiation): SSN for « Simultaneous Switching Noise » due mainly to the wires parasitic inductances **EM Field Creation**
- P/G current loops (differential mode radiation) **EM Field Creation**
- Unintentional EMI radiation by miniature antennas (lead frames, interconnections…)
- Intentional or unintentional receivers can then pick up these EM waves

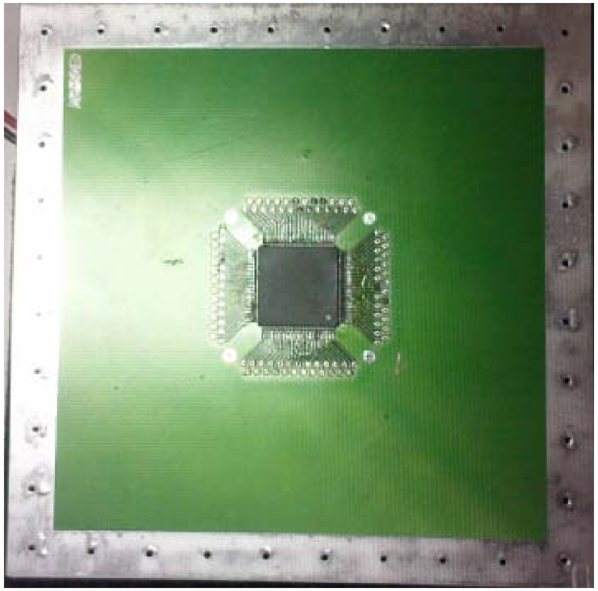


2. Background

EMI measurements:

- Based on IEC 61967-2 standard:
  - ❑ Dedicated EMI printed circuit board
  - ❑ Help of a TEM-Cell as an EMI receiver
  - ❑ Results visible on a spectrum analyzer

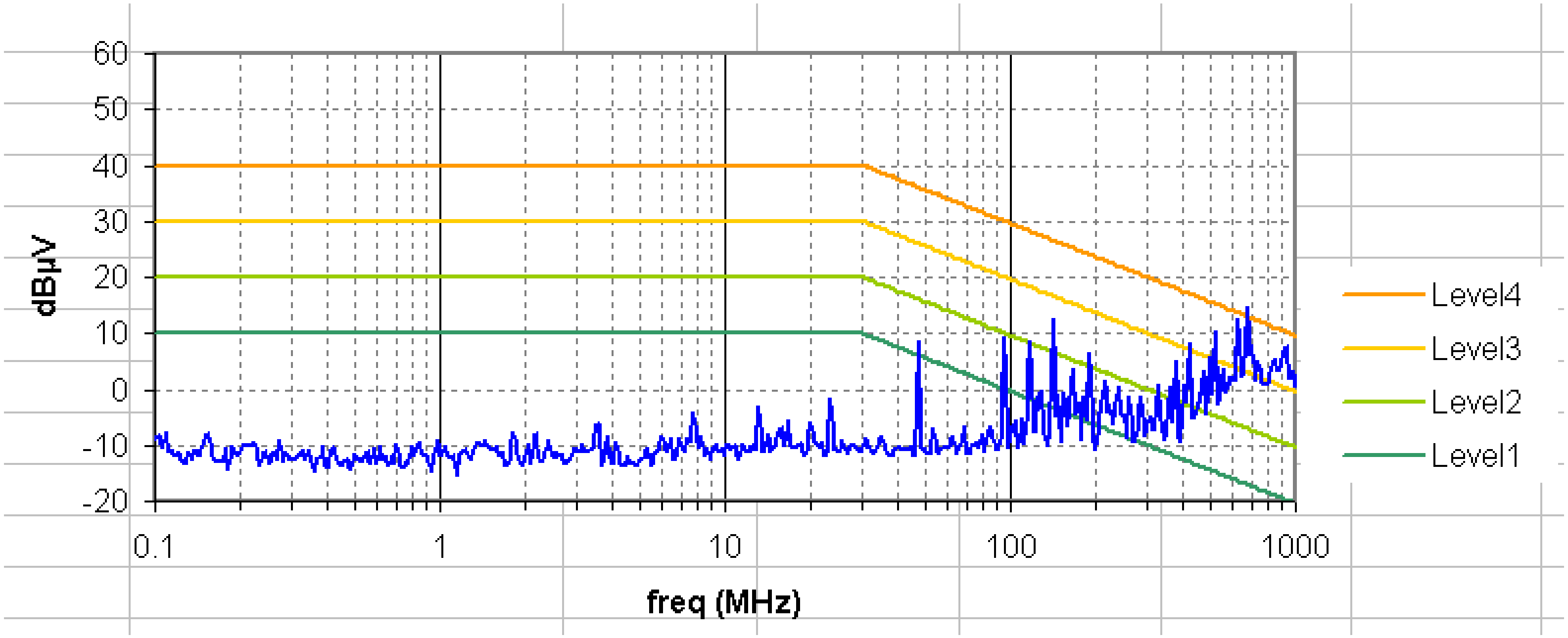




2. Background

Measurement results:

- 32-bit STXX running in **Normal** mode (f_{OSC}=8MHz & f_{PLL}=24MHz):

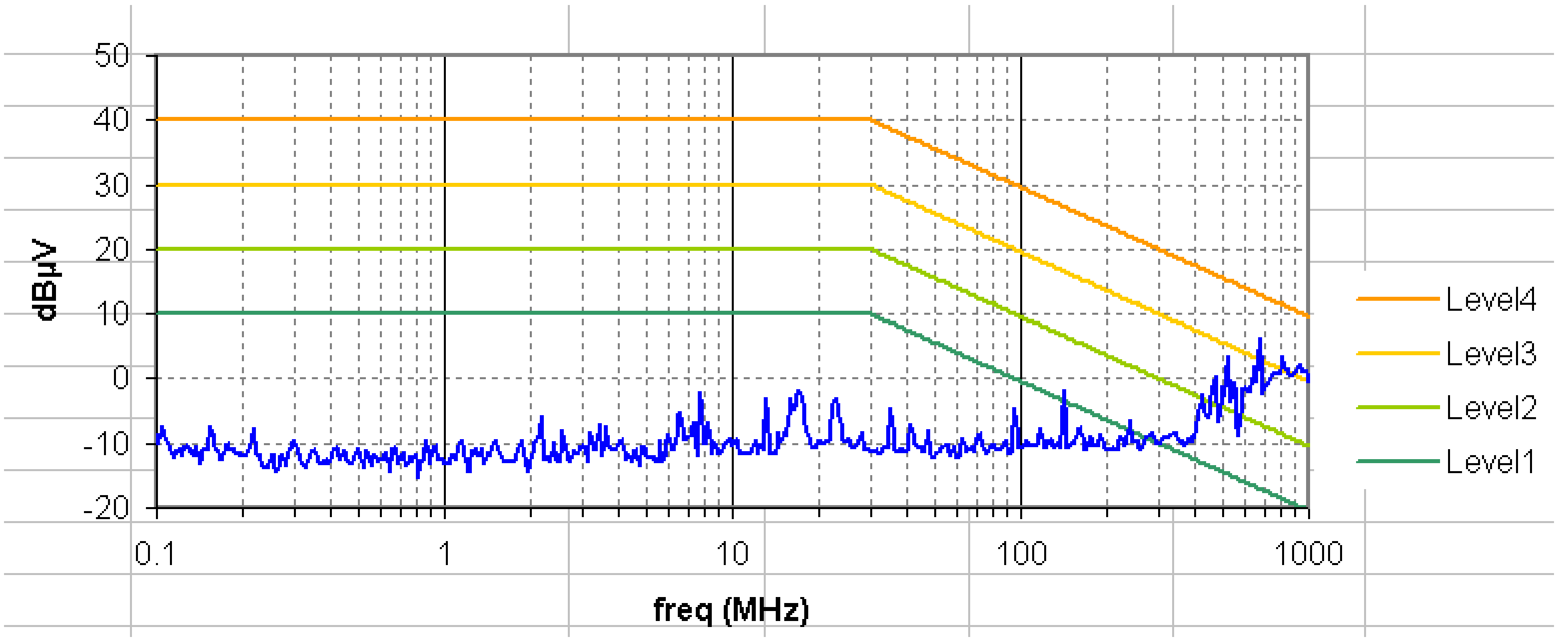


- ❑ SAE level of 5 (Not recommended in applications).
- ❑ Main CPU clock enabled and accesses to the FLASH memory.
- ❑ Resonance @ 660MHz.

2. Background

Measurement results:

- 32-bit STXX running in WFI mode (f_{OSC}=8MHz & f_{PLL}=24MHz):

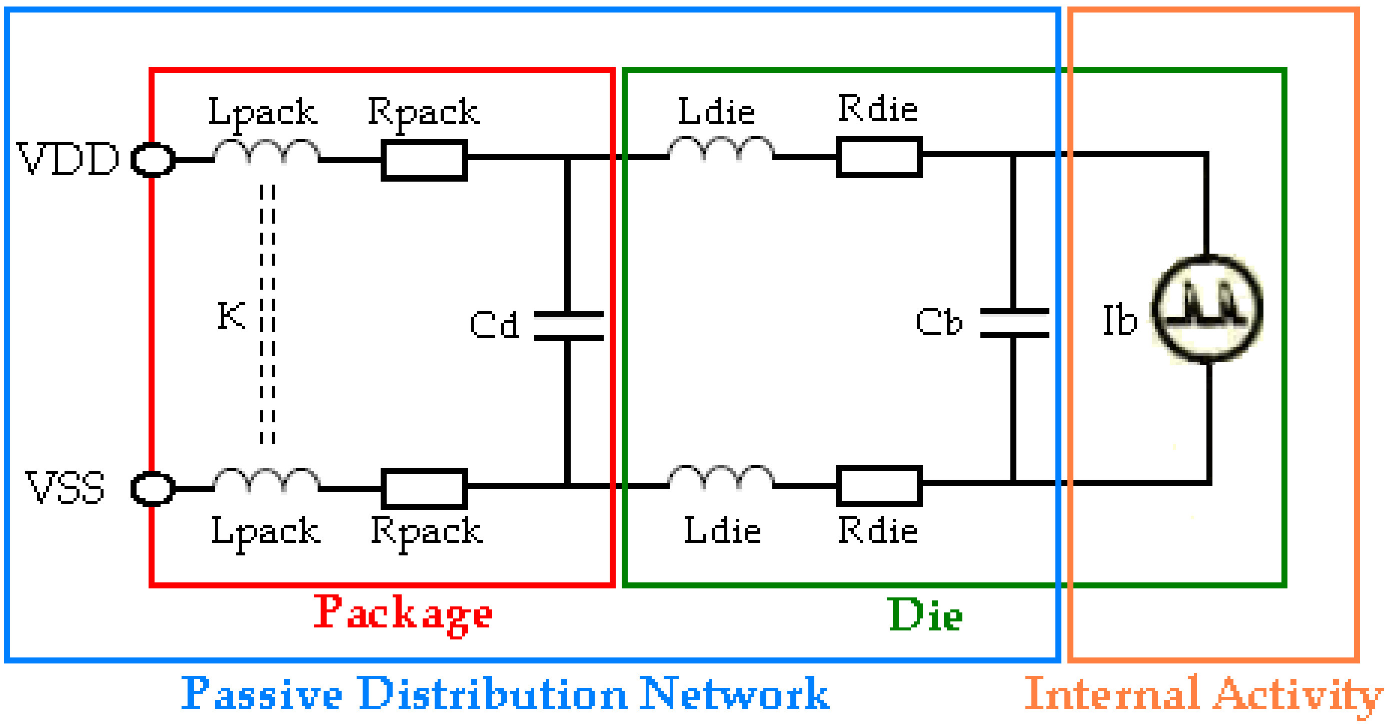


- ❑ SAE level of 4 (High EMI risk in applications).
- ❑ Main CPU clock and FLASH memory disabled.
- ❑ Resonance @ 660MHz.

3. EMI Modeling

Modeling methodology:

- Based on the ICEM, for « Integrated Circuits Emission Model ». standard (IEC 62014-3).
- Goal:
  - ❑ To predict EMI level during the design stages.
  - ❑ To test different design/layout solutions.



3. EMI Modeling

Microcontroller modeling:

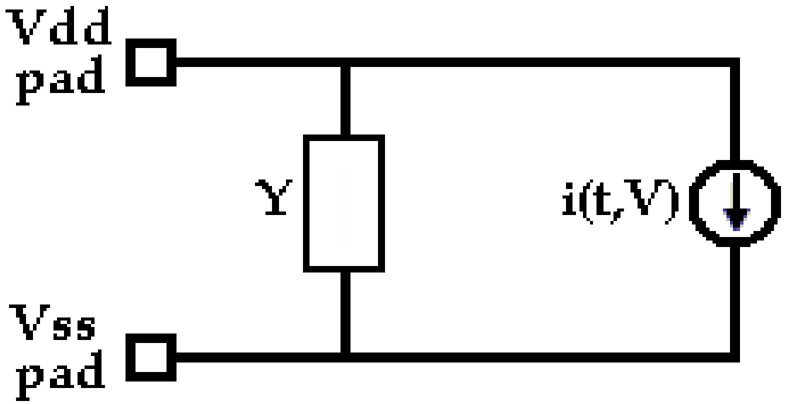
- Main noise generators:
  - ❑FLASH memory.
  - ❑1.8V Digital core.
  - ❑Crystal Oscillator, PLL, extracted clock tree.

Normal Mode

Wait Mode

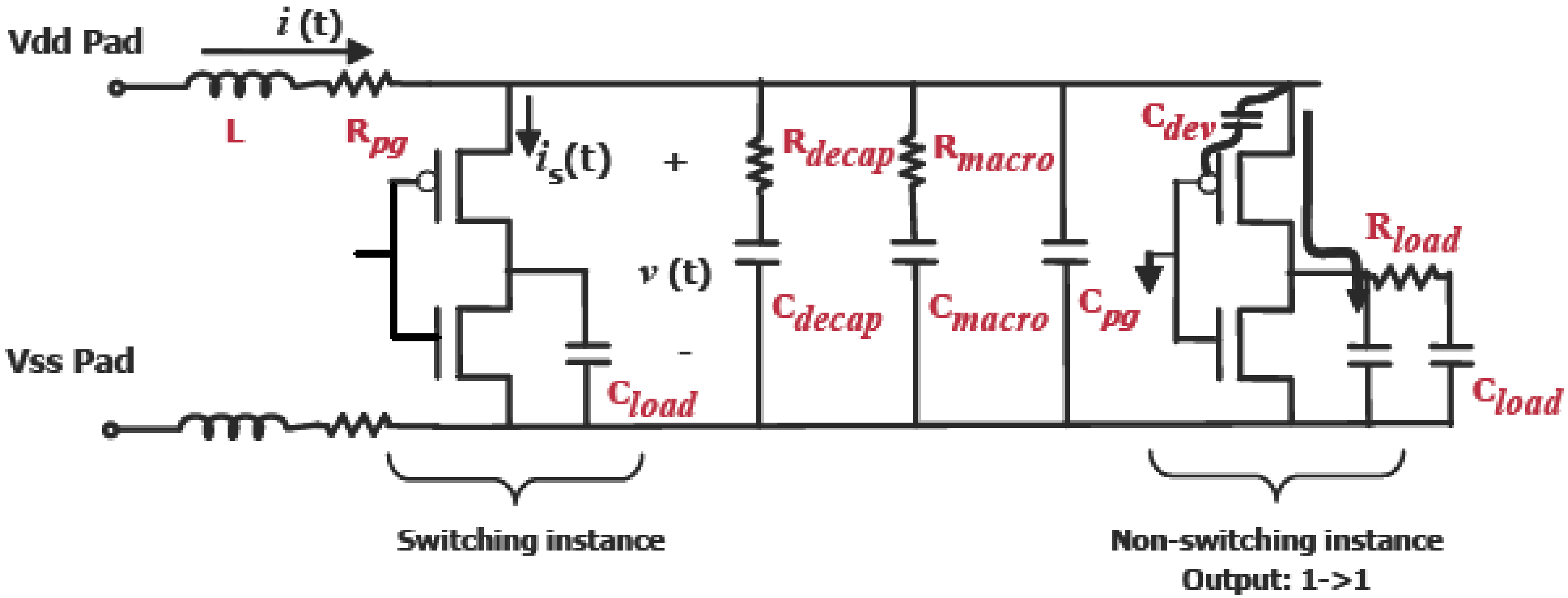
Digital Core model:

- PWL current source
- On-die admittance



3. EMI Modeling

- RedHawk-CPM Principle:
  - ❑On-chip P/G network => RLC mesh
  - ❑Switching instances => PWL sources i(t,V) after standard cells characterization
  - ❑Non-switching instance => decaps, ESR



Apache-CPM flow:

Standard Cells caracterization (current profiles and intrinsic capacitances)

↓

Import & set up design

↓

Power calculation to evaluate the average power consumption

↓

P/G RLC extraction

↓

Vectorless dynamic analysis (frequency, toggle rate, input transition …

↓

Chip Power Model (CPM) extraction

↓ ↓ ↓

SPICE DIGITAL CORE MODEL

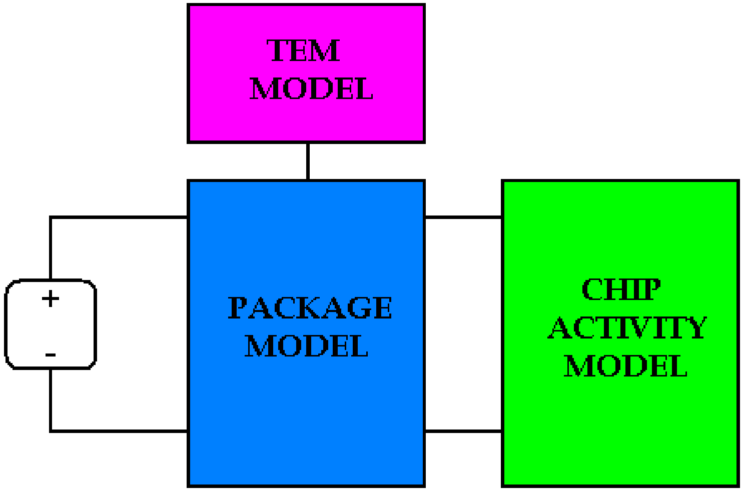
- Needs: .tech, .lib, .cdl, .gds2, .def, .lef …

3. EMI Modeling

Microcontroller WFI model:

- WFI mode: Memories and digital core disabled – Simulated Model.
  - ❑ Best case for the EMI
  - ❑ SAE level = 4
  - ❑ Modeling possible in SPICE.

- Three main parts:
  - ❑ Die model (noise generator + on-die PDN).
  - ❑ Package model (off-die PDN).
  - ❑ TEM-Cell model (receiver PDN).



3. EMI Modeling

Die model:

Noise Generator

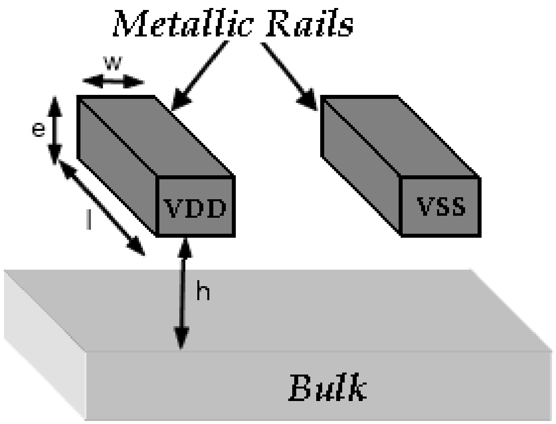
- Noise generator constituted by:
  - ❑ 8MHz crystal oscillator and 8 to 24MHz PLL.
  - ❑ 3.3V to 1.8V regulator.

On-die Power Distribution Network

- Internal capacitances between the supply rails (by estimation, post-layout extraction or simulation).
- Wires inherent inductances and resistances.
  - ❑ Tracking of the supply rails from the product gds2.
  - ❑ Inductances and resistances computation (no skin-effect and mutual inductance in this model).

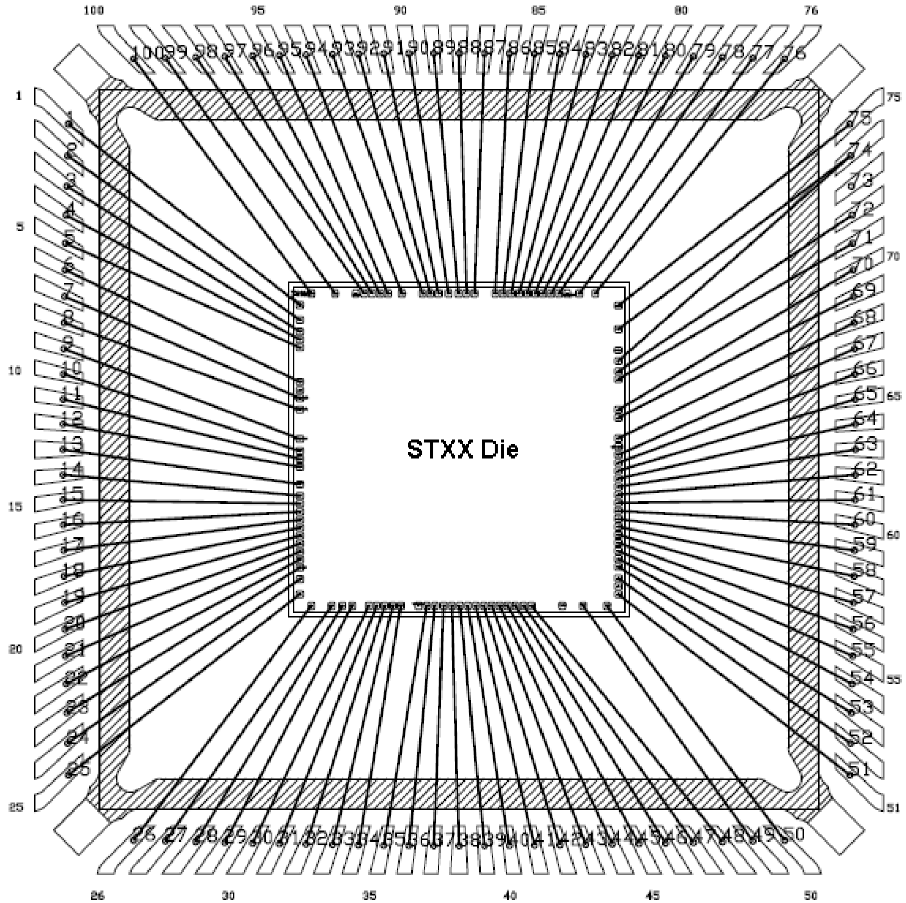
$$R_{RAIL} = R_0 \frac{l}{w}$$

$$L_{RAIL} = l \frac{\mu_0 \mu_r}{2\pi} \ln\left(\frac{4h}{w} + 1\right)$$



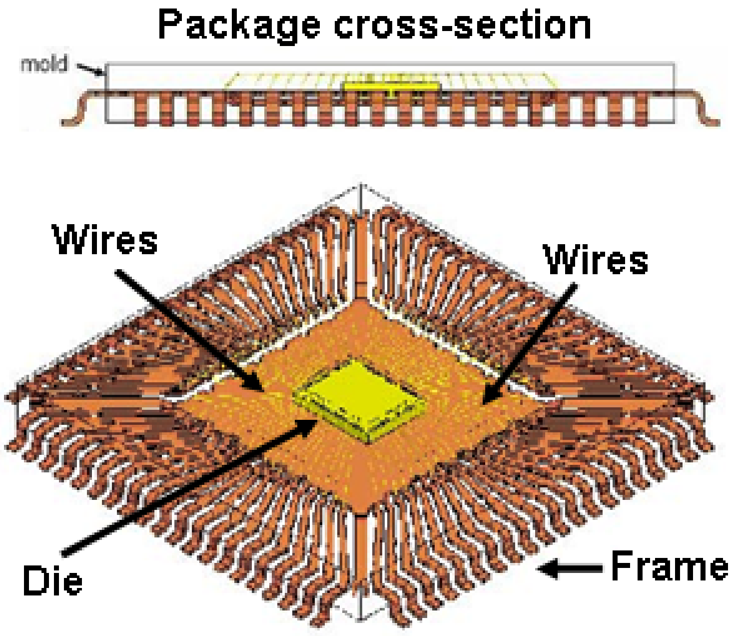
Package Model:

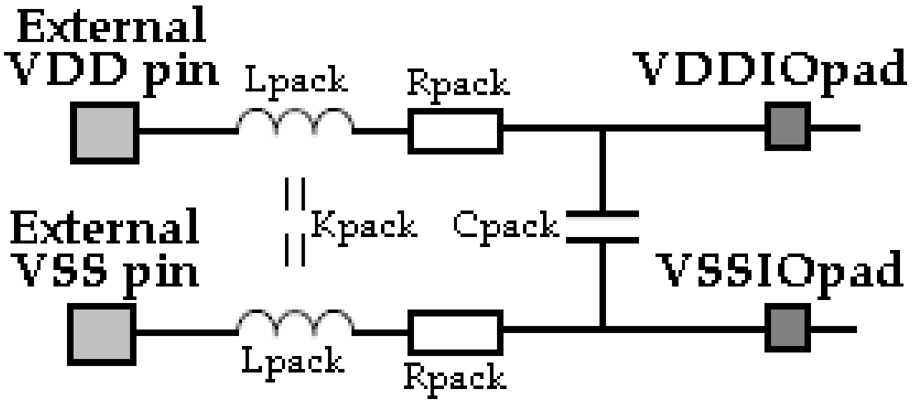
- STXX 100-pin LQFP bonding diagram:
  - ❑ Long bonding wires => important inductances.
  - ❑ Need also to add the inductance due to the lead frames.



3. EMI Modeling

- Model obtained with Ansoft Q3D and HFSS:
  - ❑Each supply couple is modeled.
  - ❑Valid up to 1GHz.
  - ❑RLCK network.

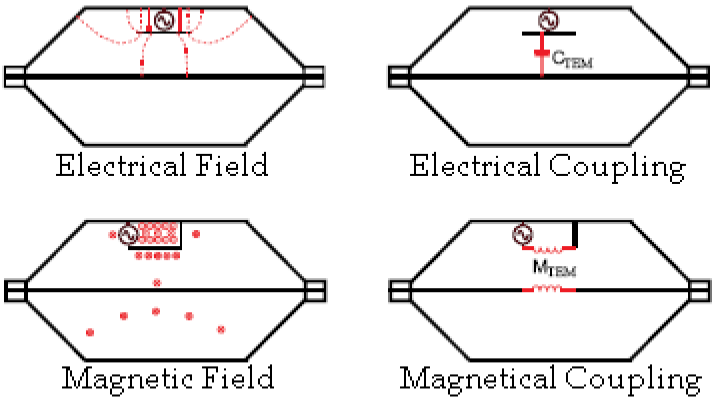


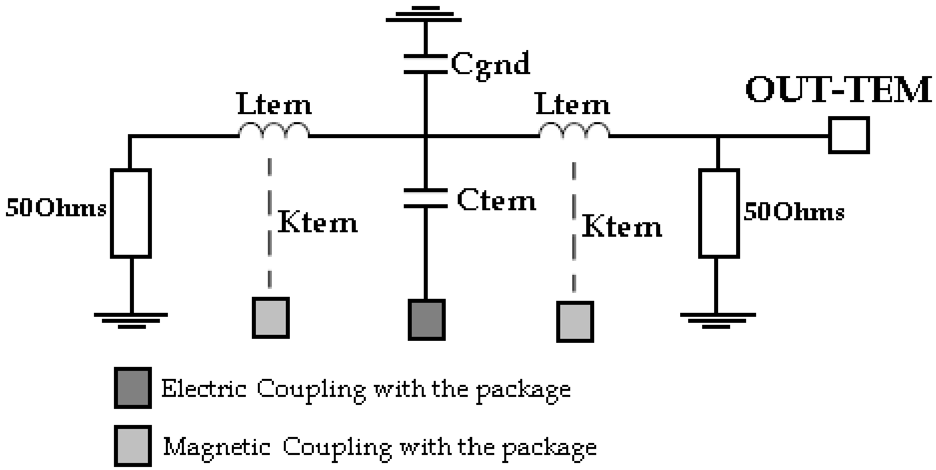


3. EMI Modeling

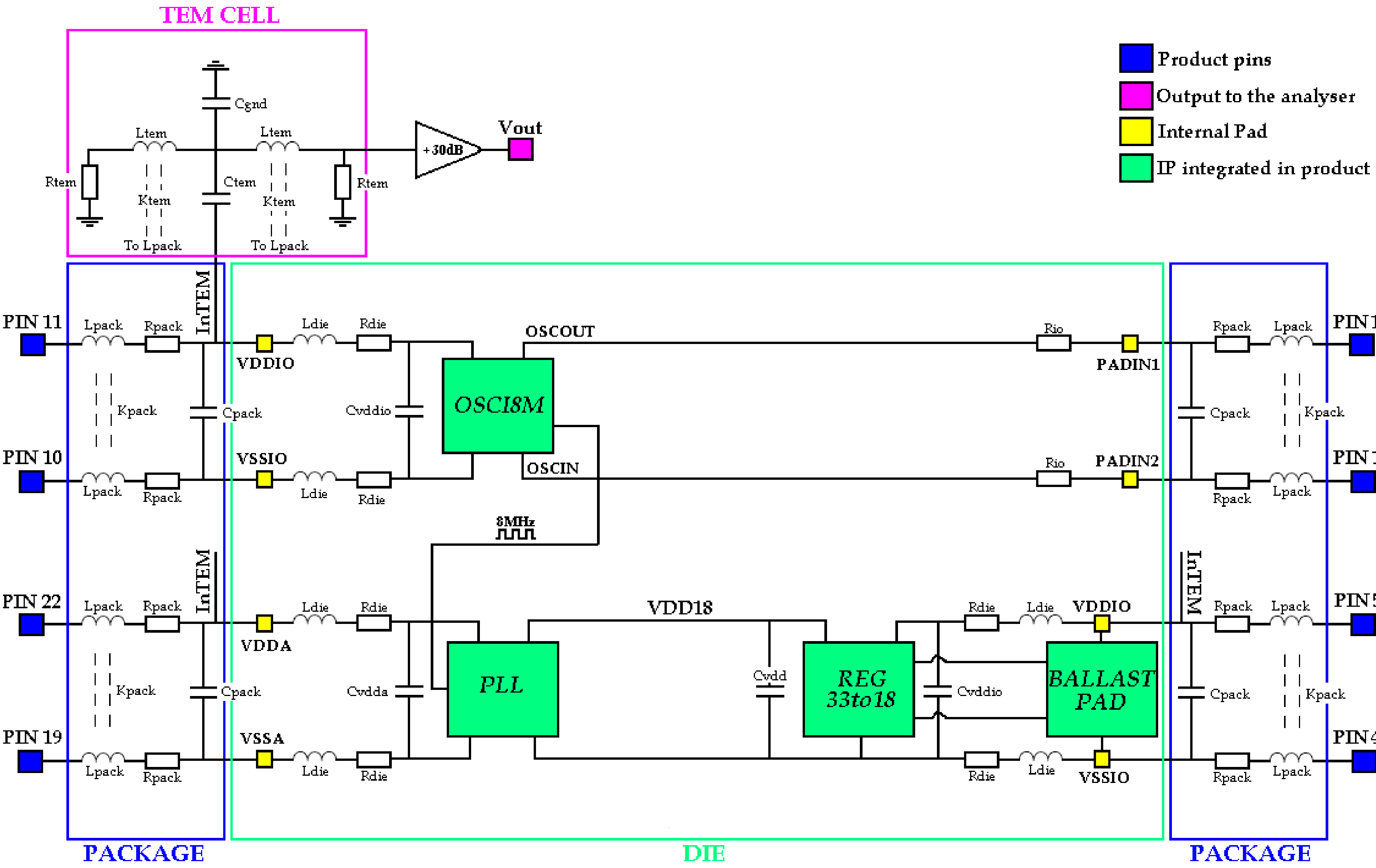
TEM-Cell Model:

- Obtained with an EM solver:
  - Representation of the electric and magnetic coupling between the chip and the TEM-Cell septum
  - Valid up to 1GHz
  - RLCK network





3. EMI Modeling



4. Results and correlation

Comments on the model:

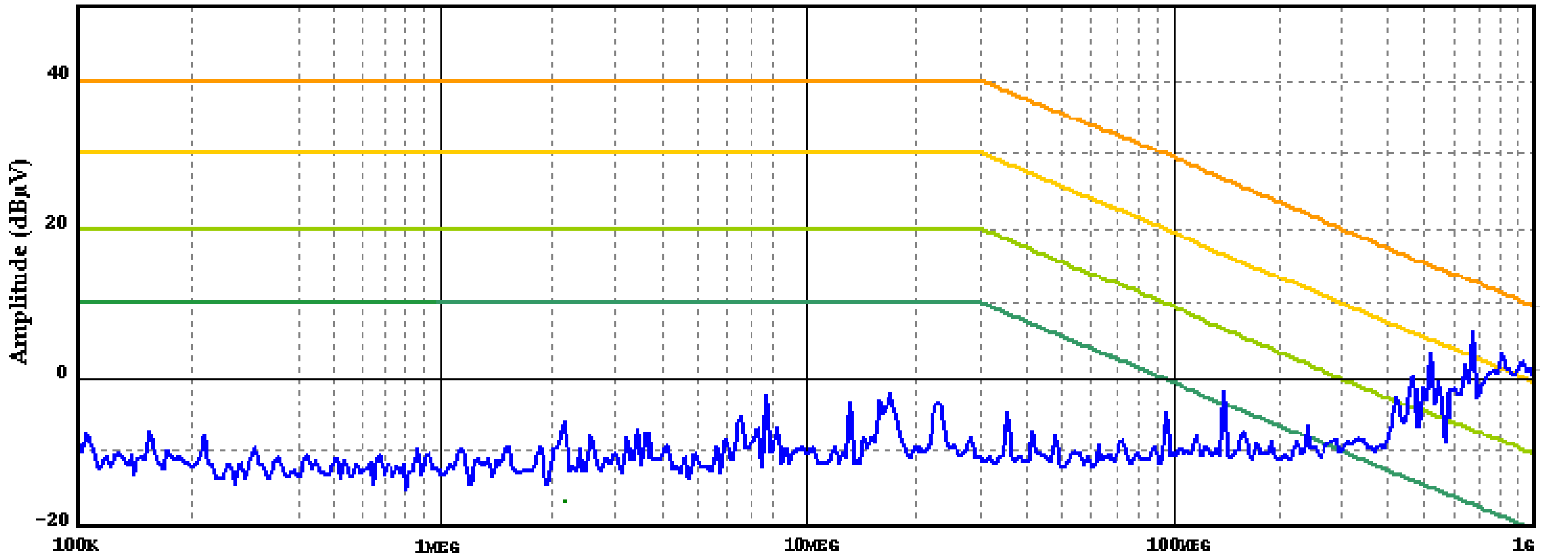
- In this model:
  - Only the voltage drops are modeled.
  - The current loops are not modeled.

- SPICE simulation with ELDO:
  - External 8MHz quartz (with its capacitances)
  - PLL with a factor x3
  - PVT conditions: Typical process, VDD_{IO}=3.3V & V_{CORE}=1.8V, T°=27°C

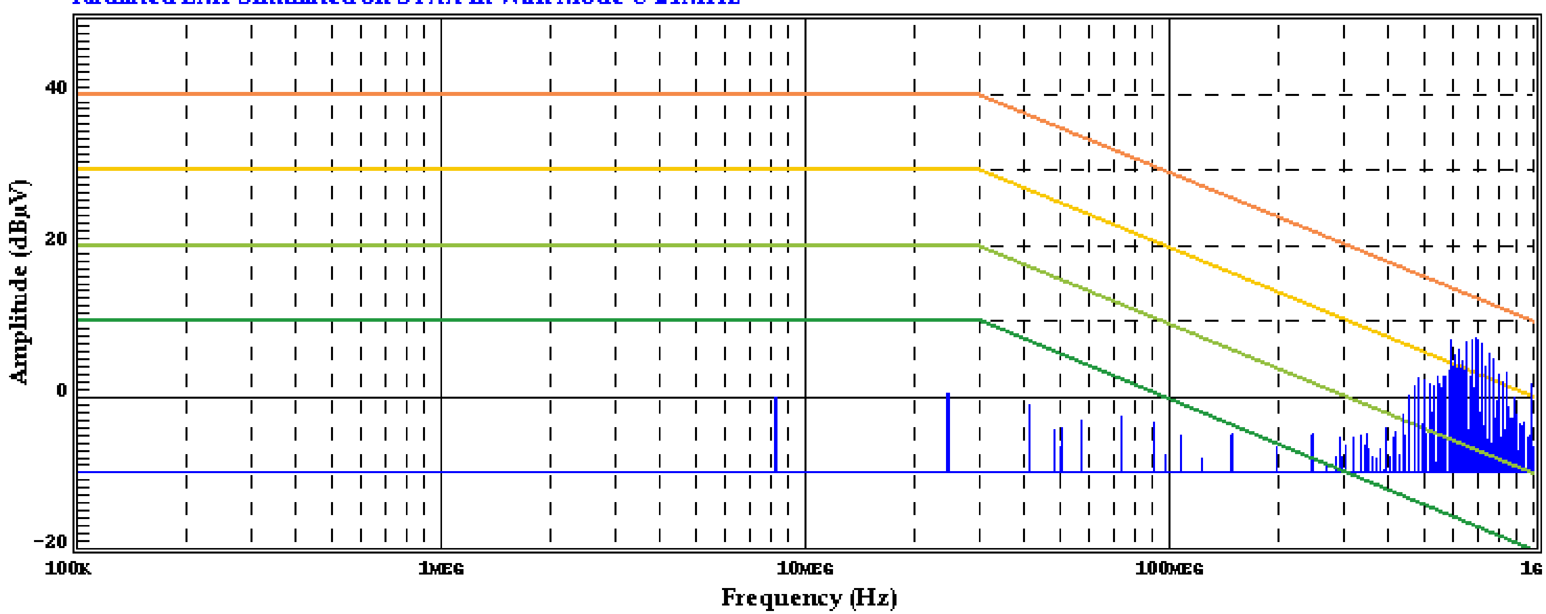
- Good correlation with WFI measurement (see next figure)
  - Similar amplitude peaks.
  - EMI at the same frequencies (harmonics + resonances)
  - Effect of the position of the chip visible.

4. Results and correlation

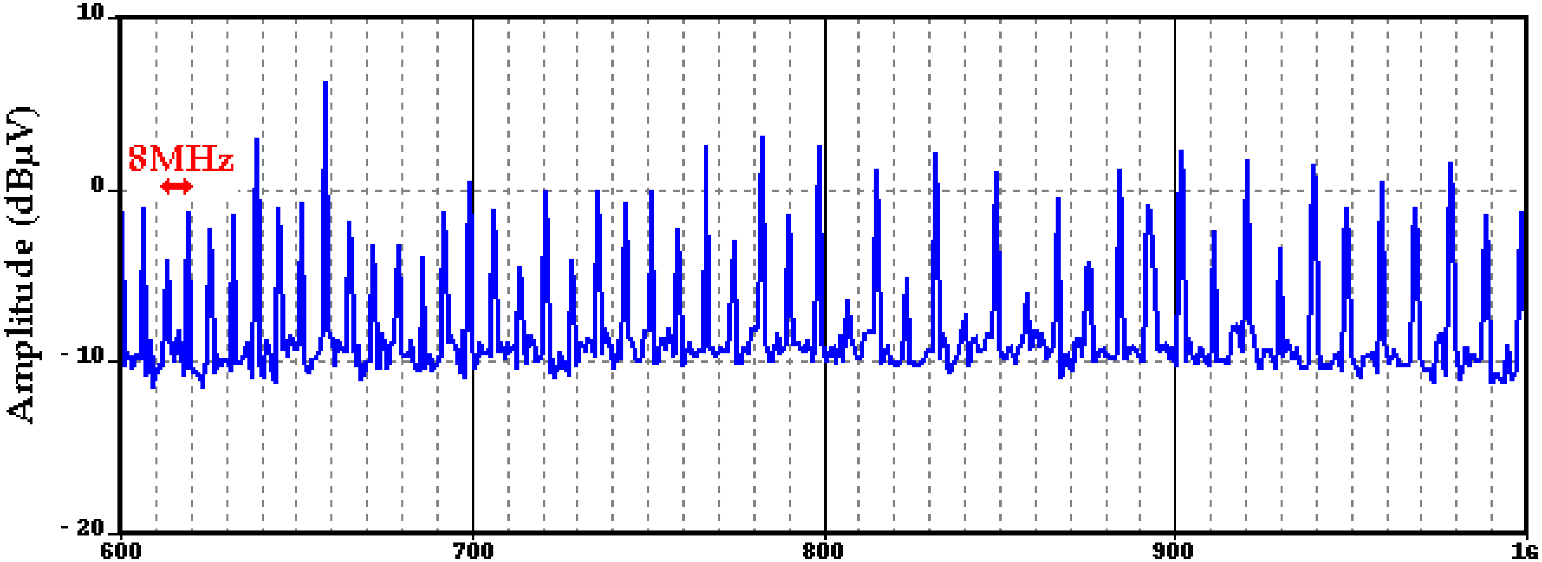
Radiated EMI Measured on STXX in Wait Mode @ 24MHz

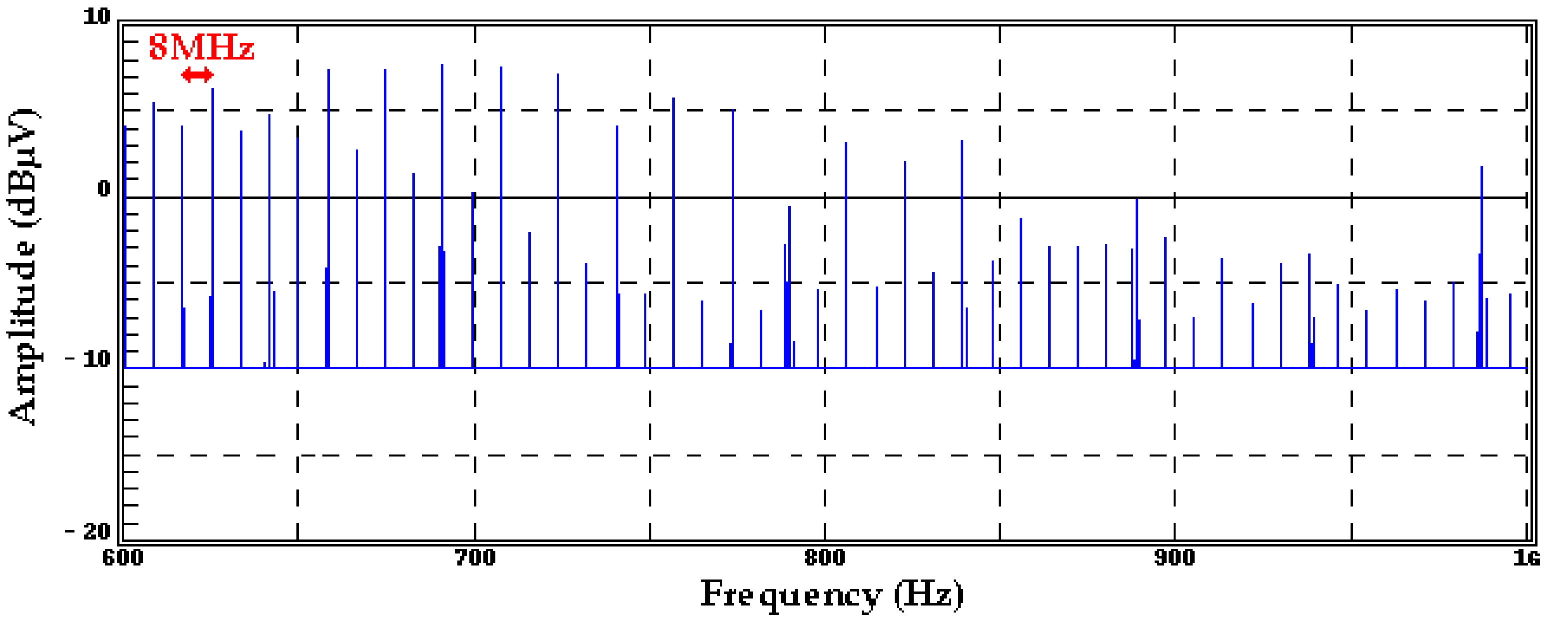


Radiated EMI Simulated on STXX in Wait Mode @ 24MHz



4. Results and correlation





4. Results and correlation

Comments:

- Resonance frequency near 660MHz:
  - Observable behavior in measurement and simulation.
  - The SSN on supplies is a damp sine wave in the time domain.
  - In the frequency domain, RLC filter effect due mainly to:
    - The package inductance
    - The capacitance between the supplies
  - Effect of the on-die resistance (Q and BW)

$$f_c = \frac{1}{2\pi\sqrt{LC}} \qquad Q = \frac{L2\pi f_c}{R} \qquad \Delta f = \frac{f_0}{Q}$$

- Conclusion: an EMI level of 4 when the chip is running in a WFI mode could be predicted during the design stage.

5. Conclusion

Performances:

- Good EMI prediction.
- Good EMI mechanisms representation.
- Quite simple to put in place.

Limitations:

- Only apply to the WFI mode.
- Long simulation time (~15 hours).

Future improvements:

- Add others running modes by modeling the digital core and the Flash memory.

Thank you for attention!